**Power Management Integrated Circuits**
**Dr. Qadeer Ahmad Khan**
**Department of Electrical Engineering**
**Indian Institute of Technology, Madras**

**Lecture – 37**
**Dead-Time Switching Loss in DC-DC Converters**

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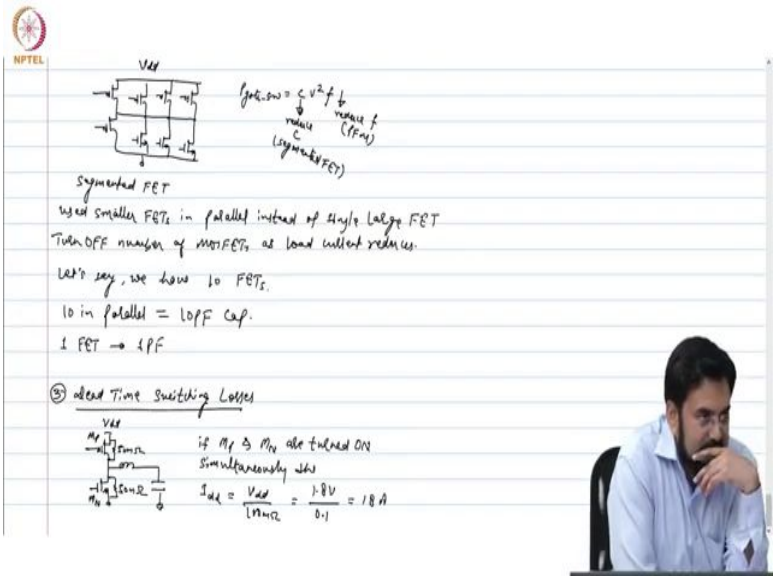


So, this is another type of switching loss which is called Dead-Time Switching Loss. So, you have this side, what would happen if I turn on them simultaneously? So, this is let us say, 50 milliohm, this side also 50 milliohm. So, if this is M P, so, if M P and M N turned ON what will be the I dd current? 18 amps.

And you have size this to derive maybe 1 amp, or 2 amp. So, 10 times more current it will break your power factor, it will damage metals, it will damage your FETs everything.

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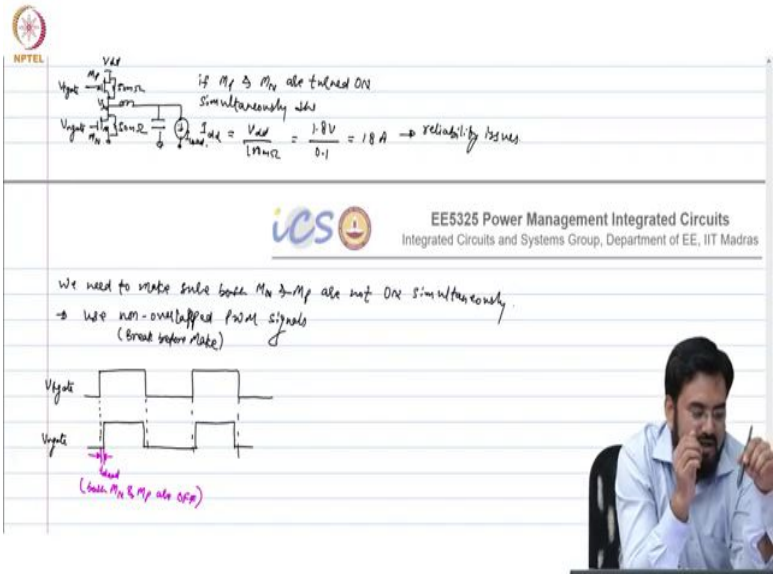


So, it means we have reliability issues due to high. So, we need to make sure both M N and M P are not ON simultaneously.

So, use non-overlapped PWM signals and you can also call it break before make which means you have to break the current switch, before you turn ON the other switch. So, let me call it V of pgate and this is generated form a single clock only.

So, we will look at the circuit how we will generate it, but these are the same: you have PWM coming from your feedback loop and you split into two non overlapped clocks, one becomes P gate other becomes N gate. So, if this is your P gate sorry V of P gate. So, this is the time actually there, FETs are OFF. So, your P gate is high, so that is a PMOS so that is OFF and N gate is low, so both FETs are OFF, and this is called t d or I will call it t dead each, both M N and M P are OFF ok.

So, when your P gate is high, the load current is flowing through PMOS sorry P gate is low your load current is flowing through PMOS and if your N gate is high or the bottom switch is ON the load current is flowing through NMOS. So, now, during this time dead time both are OFF, so where is the current going then?

So, this is your load current. So, where will the current go?

I mean capacitor will start discharging, but what would happen to the inductor and inductor other end is? Open.

Student: Then high resistance.

No, high resistance is there, but think about. All of a sudden you turned OFF both the switches, inductor will maintain the current, inductor is a current storage circuit just like capacitor is a voltage storage. So, there is a memory actually they are in the inductor, the current of inductor cannot change instantaneously it would not go to 0.

Because, it has some slope, RC time constant. So, it will rise and fall based on the voltage. So, if you leave that high impedance the other node of your or Vsw. If I call it V sw and the current is still flowing into this I mean, load current let us say 1 amp ok that was which was flowing through NMOS and you turned it OFF, you leave it, I see that 1 amp will keep flowing for certain time unless the voltage across the inductor falls to 0, current cannot be 0. So that, what where that voltage will go?

It will start going to negative and if it goes below negative voltage then based on the rating of these devices, it may even damage your device. So, this cannot go or you should not allow this to go to large negative voltage otherwise it might damage your device.

No, it will flow through the diode. There is a diode here hidden diode. Body diode I will show you. So, this is your substrate P-substrate correct, this is your n plus side body. So, if I call it source, drain, gate this is nothing but and this is your bulk B, drain, source. So, what is diode? This is your diode. So, wherever P type diffusion and N type diffusion meets that form that will form a diode.

So, how many diodes do you have here? I change the color. So, this will form N side and substrate will form P side. Another diode you have here, ok, which means, if you want to draw here those diodes. So, if P is common to both diode which is a substrate; which is your bulk or body of the so these are this is called body diode actually and in most of the cases the body is tied to the for NMOS tied to the lowest voltage for because the P type, because you do not want to forward by these diodes and for a PMOS its tied to the highest voltage because body is N type here and so, diffusions are source and drain diffusions are P type.

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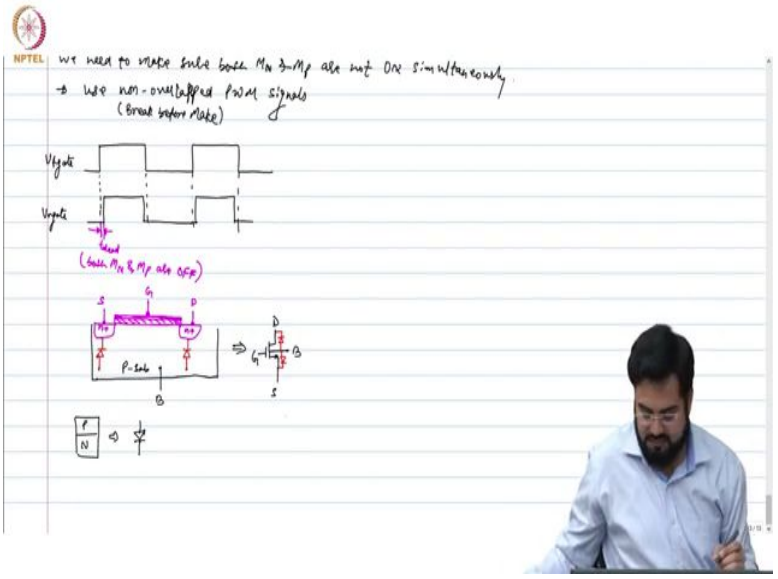


So, if you connect to the ground. So, the bottom diode will go away ok. The diode tied between bulk and source will go away, if you short bulk to the ground and source is also grounded. So, your diode left is bulk and drain.

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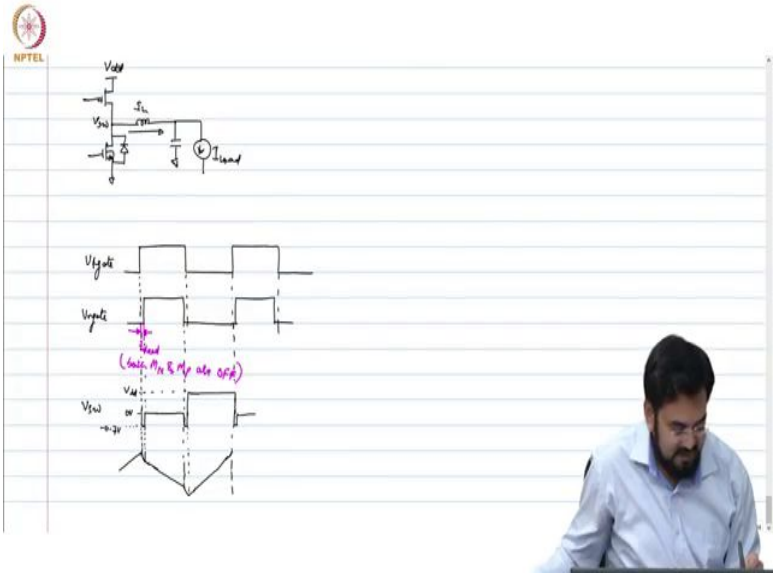


So, what you have here is so if this is tied to ground, you will get a diode here, correct, so, now if I have this waveform.

Yeah, but that will not conduct, because this will only go to negative. So, the PMOS will have a P here, so that will, always remember that will not conduct because current direction is going from this to towards load. So, this will always be negative then during dead time ok. So that diode will not conduct.

So, this is V sw. So, first let us see what would happen to the V sw. So, what would be the V sw at this, so if this is V sw where will it go? So, this is going negative.

I L, current is flowing in this direction. During dead time, current will keep flowing and this will go negative. So, the moment it goes below forward voltage this diode will conduct minus 0.7. So, it will get clamped at 0.7. So, let us say this and this will remain for the duration ON, now after this what is happening, I am turning ON NMOS, where will it go?

So, if this is minus 0.7, where will it go when the NMOS turns ON? So, let us forget about the IR loss IR drop and you can ignore that. So, it should go to the ground level 0. So, this is the 0 volt and it should remain 0 until this point and will again do the same thing. Now, what is happening after this, which device is turning ON?

PMOS is turning ON. So, it should go to V dd correct, that is the same thing. So, how the inductor current will look like, how does the inductor current look like?

So, the slope will change for a very short duration, otherwise the slope will follow the same V minus V out over L and for negative slope it will be minus V out over L. So, because what is happening here, V sw you are applying more voltage here, instead of 0 you are applying minus 0.7 here and V out remains same.

So, the inductor will see a larger voltage difference. So, the slope will be steeper here. So, let the inductor current was falling during this time. So, before this you assume that that was ON, so, it will get the peak here inductor current correct, what will happen here? You can see.

So, usually expect 0, but it would not be 0. So, there will be a sharp change and then it will start following the normal slope, correct. And then what would happen here? So, NMOS was ON, so it will first fall and then.

Infinite and again the same thing will happen after this, ok and this you can calculate from the slope that is not difficult this slope or this what are the peak value of this extra you get that can be calculated. Even though both will be negligible, but the shape will slightly change. So, now, if I assume that this ripple is very small compared to the load current then all this glitches and everything can be neglected.

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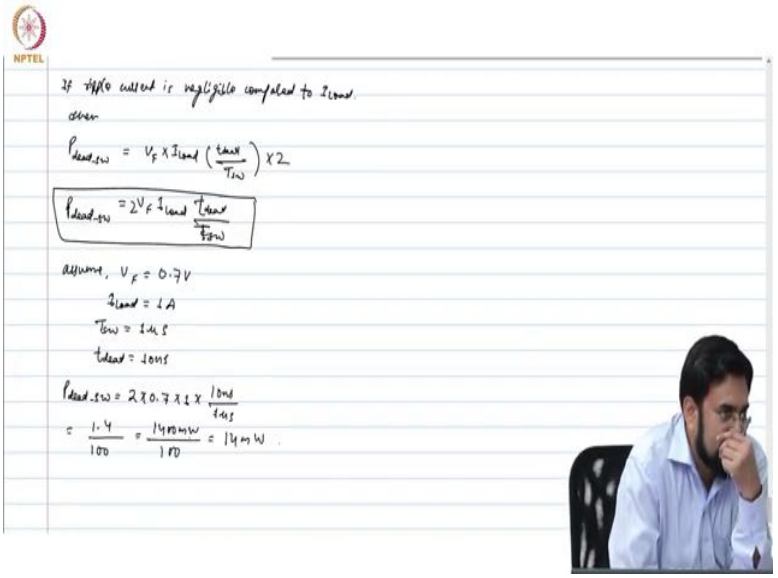


So, if I want to calculate. So, if ripple current is compared to I load then what will be the P dead? P dead switching loss, what will be that, what is the voltage? Voltage is V F, power is voltage of the diode ok minus V F and multiplied by current, how much current is flowing? How much current is flowing in the diode?

Load current and if so, this is your peak power, but this is not happening throughout the entire clock P dead. So, you have to take the average of that, so this is only happening for t dead divided by T sw and this is happening twice, this is happening at both the edges, positive and negative so, multiplied by 2.

So, approximately, so twice of V F t dead by t sw. Now, let us take an example. So, let us say I load is V F equal to 0.7 volt, I load equal to 1 amp, T sw is 1 microsecond and I will keep let us say T dead 10 nanosecond, which is 1 percent of your P dead ok. 2 into 0.7 into 1 into which is how much? 1.4.

Divided by 100, how much? So, 1400 milli divided by 14 milliwatt is ok, correct, which is quite huge. So, at 1 amp 14 milli sorry, if you are telling me let us say 1 volt power how much efficiency loss you will get? 10 milliwatt is 1 percent, 1.4 percent.

So, 1.4 percent is not a small actually ok, when you are competing with the different parts or different competitors even you try to extract even less than 1 percent efficiency of that ok. So, ideally I would like to minimize this as much as possible. So, what can I do to minimize this?

So, if you make t dead equal to 1 nanosecond then 1.4 milli watt 10 times.

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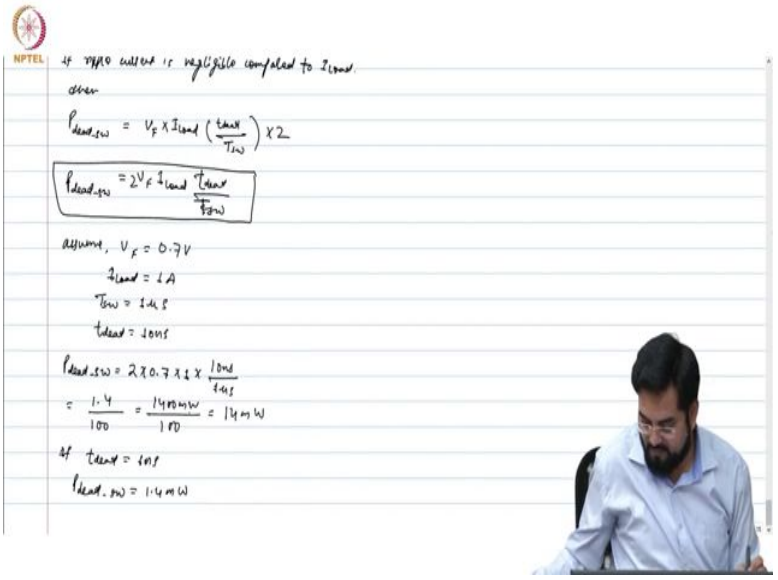


So, we should minimize t dead, increase efficiency and since this is a function of load current so, at light load it will be negligible, but at mid and high load is nearly significant enough to reduce your efficiency.

So, ideally we should try to keep it as low as possible, but we cannot keep it 0; obviously, ok. So, and because at any this kind of instant, we should not allow the 2 FETs to conduct simultaneously. So, we have to have some dead time, but we have to minimize it and since this dead time may vary across your process voltage and temperature. So, we always look at the worst case actually.

So, let us say for the worst case you design at 1 nanosecond at the other cases it may reduce actually. So, let us say you are going at a fast corner then your delays will reduce so that, 1 nanosecond may further shrink, it may go to half a nanosecond also. So, across all the corners you have to make sure that those 2 FETs should not conduct simultaneously.

If you ensure that across pvt then you always try to keep it as low as possible and there are some adaptive dead time circuits also, where they keep track of that dead time. And you keep changing the delay and in your non-overlapped clock generator to ensure a fixed time.

So, let us say you are happy with 100 picosecond and if we maintain that 100 picosecond across all pvt which ensures that your power FETs will not turn on simultaneously then that will always lock that dead time at 100. And since if that can be done using a like the PLL kind of a circuit or there are some other circuits also we talked about that later when we look at the different techniques to improve the efficiency ok.