Power Management Integrated Circuits
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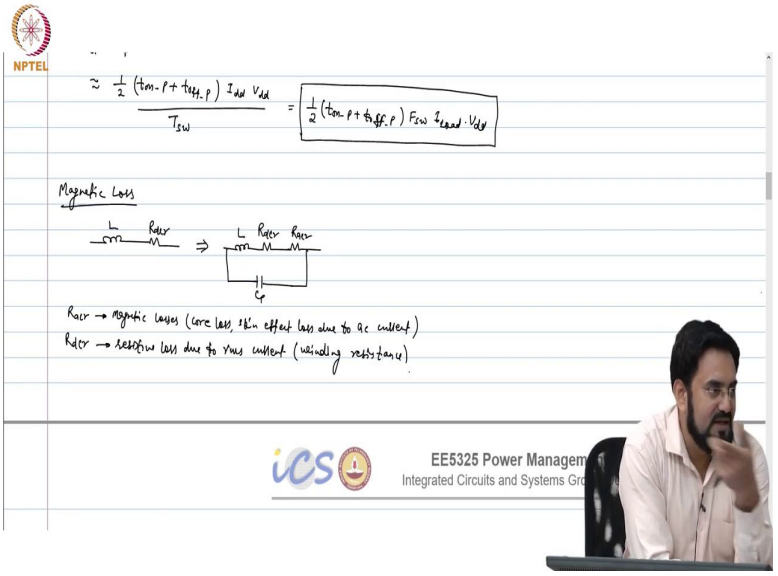
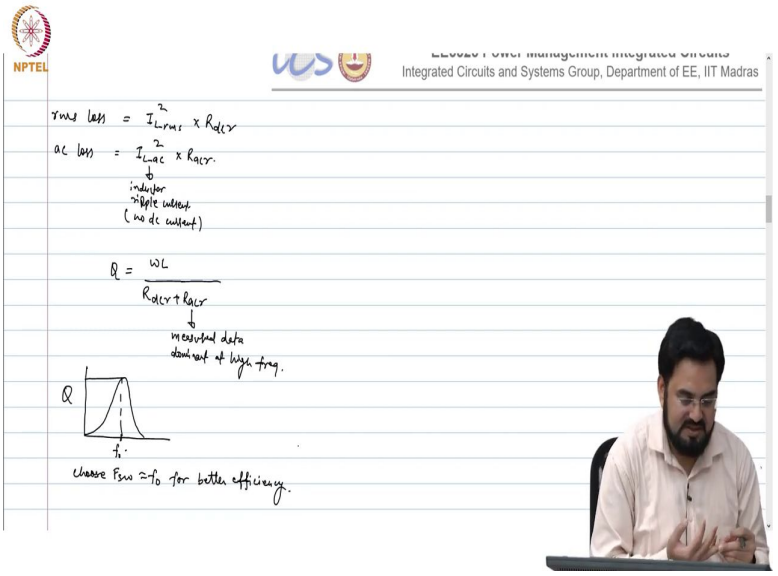
Lecture - 39
Magnetic Loss in DC-DC Converters, Relative Significance of Losses as a Function of the Load Current



The magnetic component in the DC-DC converter is an inductor. So far we have considered only the DC model of inductor i.e. only R_{dcr} in series with L, but in reality, this is not true. AC model is the actual model which is shown in the above image. AC model will have one more resistance R_{acr} and it will also have parasitic capacitor C_p. This is the actual model of the inductor when you start considering magnetic losses. R_{acr} represents magnetic losses, which are your core loss and skin effect loss due to ac current and R_{dcr} represents resistive losses.

Measuring R_{dcr} is very easy; we can simply use the ohmmeter or insert some DC current and look at how much voltage it is dropping across that. But calculating R_{acr} is not simple, you have to have ac current flowing into the inductor. And we know that there are ripples in inductor current in DC-DC converter which contributes to the ac losses.



Rms loss and AC loss are :

$$\textbf{rms loss} = I^2_{L-rms} R_{dcr}$$

$$\textbf{AC loss} = I^2_{ac} R_{acr}$$

I_{ac} is inductor ripple current. Rms loss has both ripple component and dc component, but ac loss you only have a ripple component. Larger ripples result in more ac loss.

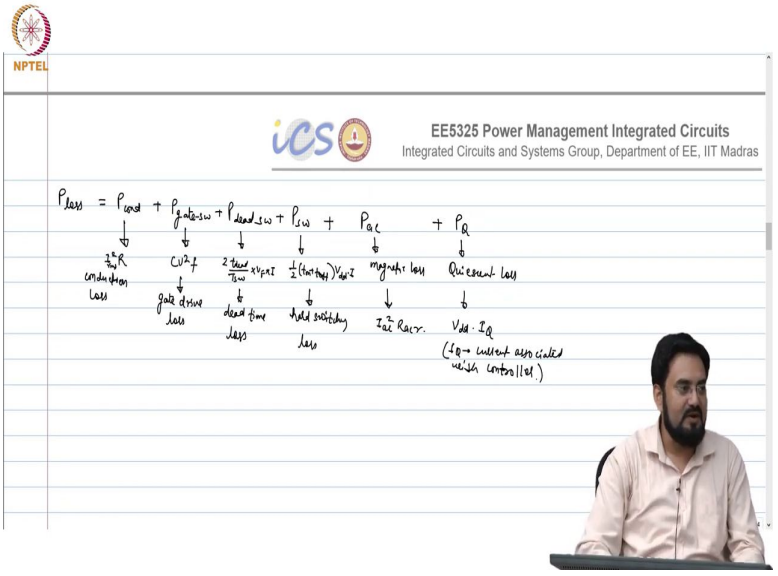
Q of the inductor is :

$$Q = \omega L/(R_{dcr} + R_{acr})$$

If Q is less than losses will be high, the inductor will be poor. Q defines how lossy your inductor is. We usually want very high Q which means we have to minimize R_{dcr} and R_{acr}. So, let us say we are using inductor which has a very negligible R_{dcr}, but if R_{acr} is very high, then choosing the inductor with a very low R_{dcr} may not help much in that case because we know there are ripples in the current and which may contribute to this core losses more and it will kill your efficiency.

R_{acr} depends on your switching frequency and usually is not given in the datasheet. We have to measure the R_{acr} by characterizing the inductor with the ac current and then measure the ac losses. R_{acr} is dominant at high frequency. Some of the data sheets may give you the Q and its plot vs frequency may look like a bandpass filter. So, wherever you have the Q of the

inductor peeking, you choose the switching frequency according to that or if you have already selected F_{SW}, then you pick the inductor which gives you the highest Q around that frequency so that you can get better efficiency.



The total loss in DC-DC converter is the summation of conduction loss, gate drive loss, dead time loss, hard switching loss, magnetic loss, and Quiescent loss.

$$\mathbf{P_{LOSS} = P_{COND} + P_{gate\text{-}SW} + P_{dead\text{-}SW} + P_{SW} + P_{ac} + P_Q}$$

$$\mathbf{P_{COND}} = I_{rms}^2 R$$

$$\mathbf{P_{gate\text{-}SW} = CV^2f}$$

$$\mathbf{P_{dead\text{-}SW} = 2(t_{dead}/T_{SW})V_F I}$$

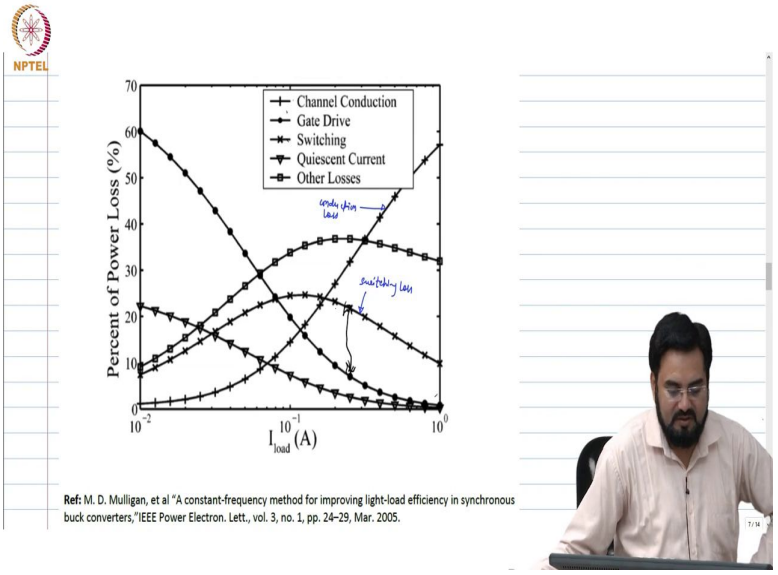
$$\mathbf{P_{SW} = 0.5*(t_{on} + t_{off})V_{dd} I}$$

$$\mathbf{P_{ac}} = I_{ac}^2 R_{acr}$$

$$\mathbf{P_Q = Vdd*I_Q}$$

I_Q is the current associated with the controller. We have a controller in the feedback which consists of components that require current such as bandgap, comparators, error amplifiers,

etc. At light load, one way to improve efficiency is by reducing the switching frequency. Gate driver loss, dead time loss, and hard switching loss will go low on decreasing the switching frequency and conduction loss is already low because we are not operating at very high load but this I_Q will be fixed and it is not going to change because the controller is on. P_Q will start dominating at very light load and will determine the efficiency. We try to design our controller with a very low current.



The graph in the above image shows the normalized loss which means it tells the percentage of each loss at different load currents.

At a very high load, conduction loss will start dominating and that is what you see in the graph. As current is increasing, the contribution of conduction loss is getting higher compared to the rest of the losses. Switching losses (hard switching loss and dead time switching loss) will also increase on increasing the load current but the rate of increase of conduction loss will be more because conduction loss is proportional to the square factor of load current whereas switching losses are proportional to load current. Gate drive loss and Quiescent loss are fix losses because they do not depend on load current.

At light load gate drive losses are dominant and we can reduce them by reducing F_{SW}. We should know at what load current which loss will be dominant and that is how we improve efficiency by taking a proper step in the design.

At very light load, there is also a possibility that you can reduce the I_Q by reducing the controller current using dynamic biasing. We know that the switching frequency is not high at light load. So, we do not a very fast comparator and fast amplifier at that point. We can reduce the bandwidth or speed of the comparator by reducing the current and can achieve some extra efficiency at light load.