Power Management Integrated Circuits
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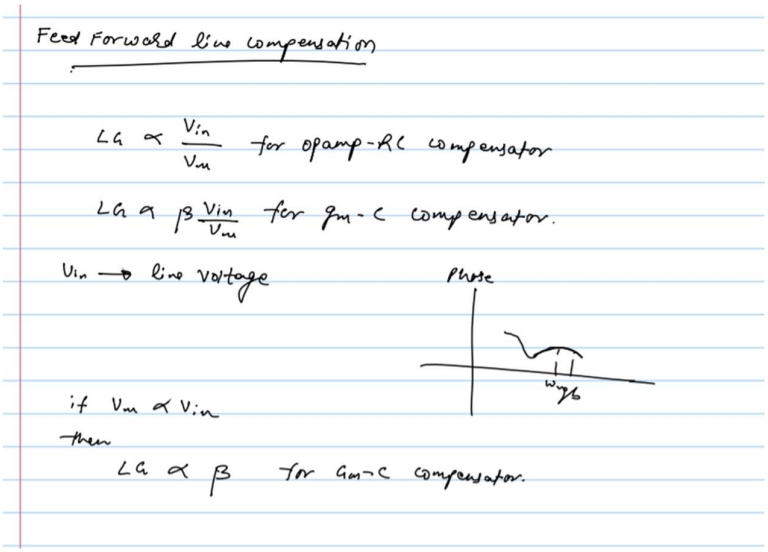
Lecture - 60
Free-Forward Line Compensation, Loop Gain Compensation by Modulating Gm

If you remember your loop gain (LG) is proportional to $\frac{V_{in}}{V_m}$ for opamp-RC compensator and it is proportional to $\beta\frac{V_{in}}{V_m}$ for g_mC compensator. So, higher line voltage (V_{in}) means your loop gain is also higher.

Let's say you have designed your compensator for one particular V_{in}, let us say 1.8 V. Now, if your V_{in} goes to 3.6 V then ω_{ugb} will be shifted at 2x. Let's say you have designed for phase margin of 55° or 60° at 100 KHz. But now your f_{ugb} has shifted to 200 KHz. If you remember your phase was dropping and it has a curvature kind of a behavior as shown in below figure.



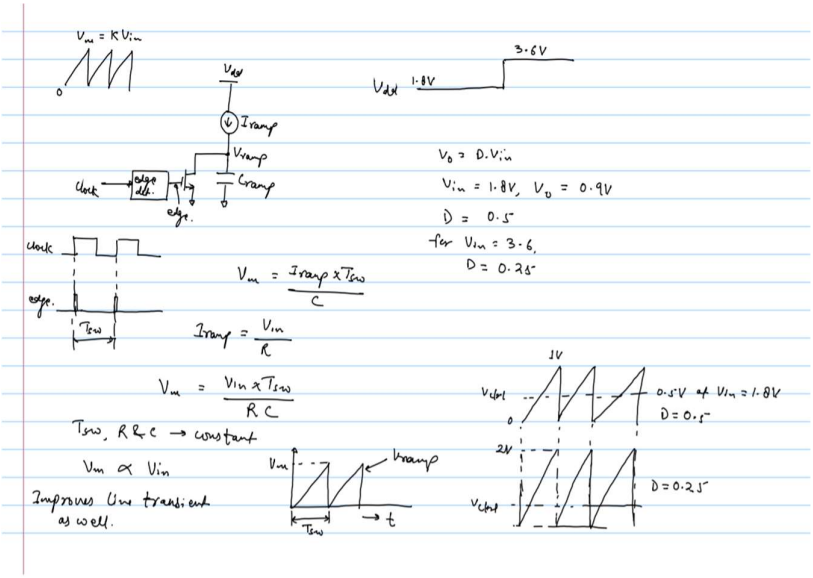
If this phase curve remains flat for a larger range of frequencies, then even 2x you may still see a good phase margin, but that is not necessary. It all depends on the shape of your phase response. So, at 2x it is quite possible, maybe 5° or 10° less and on top that if you consider the tolerances in L and C, and then other tolerances might be coming from your on-chip compensation also. It will have some variation across process, voltage and temperature. So, your phase margin may degrade even more than 10° and you do not want phase margin looking like a 45° or so. So, your 55° or 60° may look like 45° which is bad actually.

So, once you have designed it for f_{ugb} of 100 KHz, you want your f_{ugb} around that only. If you reduce f_{ugb} then your transient response will be bad because your loop will not respond to any load transient or line transient. And if you increase f_{ugb} then your phase margin will reduce. So, how can we compensate this? We have to reduce or eliminate the effect of this V_{in}. How can we cancel the effect of V_{in}?

Student: We can derive V_m from V_{in}.

Yeah, if you derive V_m from V_{in} then they will cancel out. If V_m is proportional to V_{in}, then loop gain is only proportional to feedback factor(β) for g_mC compensator. And β will only change, if you change the output voltage; otherwise β will not change. So, for a fixed output voltage, you will not see any variation when your input supply is changing.

The circuit diagram is shown in below figure to make V_m proportional to V_{in}.



The advantage with feed forward line compensation is it improves your line transient. If there are any fast changes in V_{in}, those changes will get reflected in your duty cycle immediately and it will not change your output. So, line transient is very good.

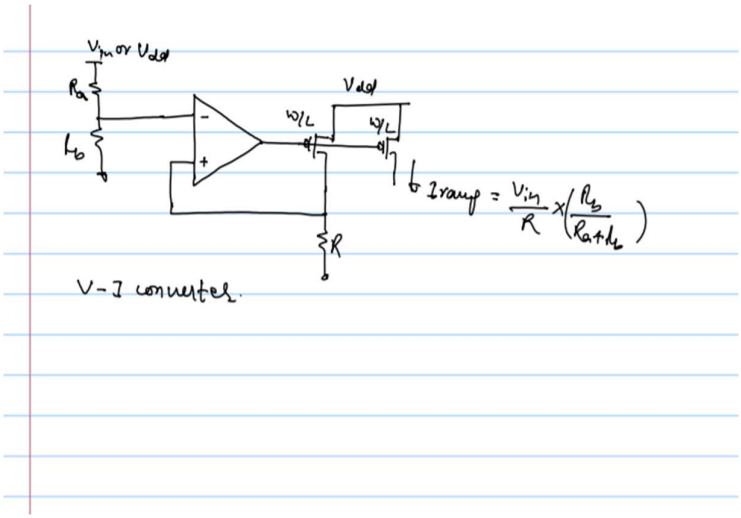
For example, your line voltage V_{in} or V_{dd} changes suddenly from 1.8 V to 3.6 V as shown in above figure. Let us say V_{in} is 1.8 V and V_{out} is 0.9 V. So, duty cycle is 0.5; forget about the losses here.

When V_{in} changes from 1.8 V to 3.6 V then D is 0.25 which means you have to go from 0.5 to 0.25 duty cycle. And duty cycle can only be changed by changing the control voltage. So, it has to go through the entire feedback. So, your control voltage will take some time to go from 0.5 to 0.25. But here, we are changing the ramp signal slope. When you are changing the ramp signal you are completely bypassing the compensator because this ramp signal is after your compensator. Let's say V_{ramp} was from 0 to 1 V and your V_{ctrl} was 0.5 V at V_{in} equal to 1.8 V.

When V_{in} goes to 3.6 V; since we are making V_m proportional to V_{in}, now ramp go to 2 V. If it goes to 2 V, then we will get duty cycle as 25%. So, when your line voltage has changed, that change will get reflected immediately in your current (I_{ramp}) and the slope of the ramp will change. Now, ramp signal will try to charge to 2 V instead of 1 V when V_{in} is increased to 3.6 V.

Student: How I_{ramp} will be controlled?

You have to design a current reference which will be a function of V_{in} . One way to design current reference is shown in below figure.



For opamp-RC compensator, you just use this particular feed forward compensation. But for g_mC, how do we do that? You have another factor β.

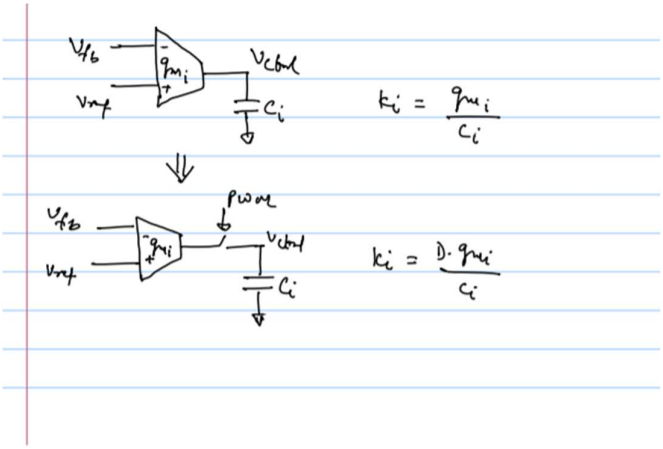
Student: β is constant.

β is constant if V_{out} is not changing but usually you do not design for a fixed voltage. These converters are supposed to be designed for wide range of output voltages. So, both input and output are changing.

For g_mC compensator, loop gain (LG) $\alpha \quad \beta\frac{V_{in}}{V_m} = \frac{V_{in}}{V_m} \text{ x } \frac{V_{ref}}{V_o} = \frac{V_{ref}}{V_m} \text{ x } (\frac{1}{D})$

If V_{ref} and V_m are constant, then for g_mC compensator loop gain is inversely proportional to duty cycle(D). So, how can we compensate this? One possibility is you can do it digitally. You measure the duty cycle with higher frequency clock. How many cycles of higher frequency clock you get in one particular on-time or off-time, and from there you can use that code to control your proportional gain. We know that proportional gain (K_p) is g_mR_P; you can change g_m or you can change R_P. So, this is one way.

What could be the other way, if I want to do it in an analog way? So, consider the g_mC integrator which is shown in below figure. So, integral gain $K_i = \frac{g_{m_i}}{C_i}$.

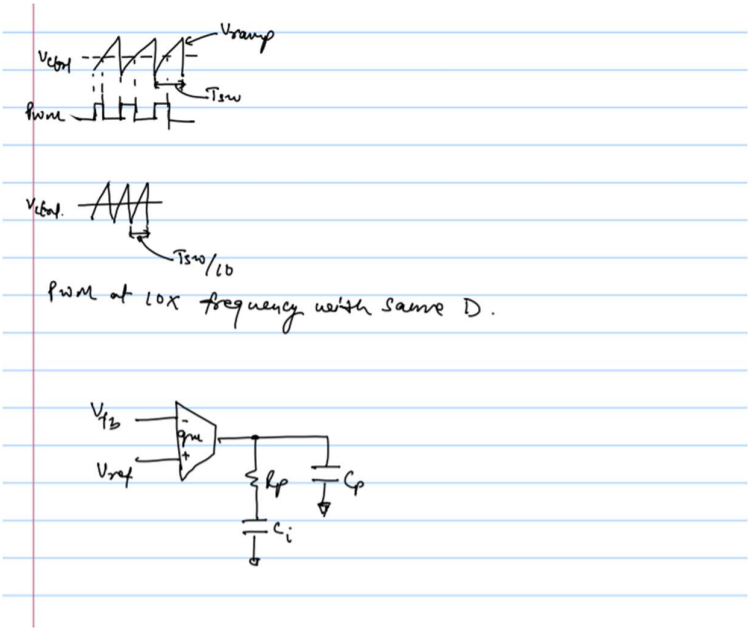


If I modify this g_mC integrator, let's say I have put a switch, and this is controlled by your PWM as shown in above figure. Then integral gain will be $K_i = D\frac{g_{m_i}}{C_i}$.

So, the effect of duty cycle will be zero in your loop gain. So, there will be no affect as such. But the clock which is controlling this switch has to be high frequency. So, one thing you have to make sure that this should not cause a ripple at the output. Since it is only integrator, so even if you use the same clock which is coming from PWM, you may not see a ripple at output.

But once you have a resistor to have proportional gain, then you may have a problem. Every time you turn on and off this switch, you will see a change in the proportional component and that will get reflected into your V_{ctrl}. Which means I want to retain the duty cycle, but run this clock let us say 10 times of F_{sw}.

Let's say I have a V_{ctrl} and this is your V_{ramp} with time period T_{sw} as shown in below figure. So, this will give your PWM with duty cycle(D). Now, if I take another ramp and the period of this ramp is let us say 0.1 T_{sw} and if I have a same control voltage, then it will simply change the frequency but retain the duty cycle. So, you get PWM and higher frequency clock with same duty cycle(D). This is the one way you can do it. But if you have only integrator, then you may not need to do all these things and you can directly use PWM signal to control the switch.



If you remember we need a small capacitor (C_p) here. The pole due to this C_p is at $\frac{1}{R_pC_p}$ and it is outside your ω_{ugb}. And it will be closer to your switching frequency. If you want your output ripple to be suppressed with this C_p, then the frequency which is modulating your g_m with should be much higher. This high frequency clock will modulate your g_m, in order to compensate for the variation in loop gain due to duty cycle. That's why choosing a higher frequency clock would be better, so that we can get all the ripples filtered out at that frequency and the only ripple left will be at your switching frequency.