Photonic Integrated Circuit
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Lecture 47
Fabrication Process - 2

Hello, everyone, let us continue our discussion on the patterning. So, we looked at lithography process where we transferred our design from the mask onto the photoresist. So, now we have to take the structures from the photoresist and transfer into silicon by using dry etch process. So, we use dry etch process because this is a standard CMOS process we use for patterning, which is much much better and controllable than other wet etch processes that we have. So, let us look at the dry etch process now.

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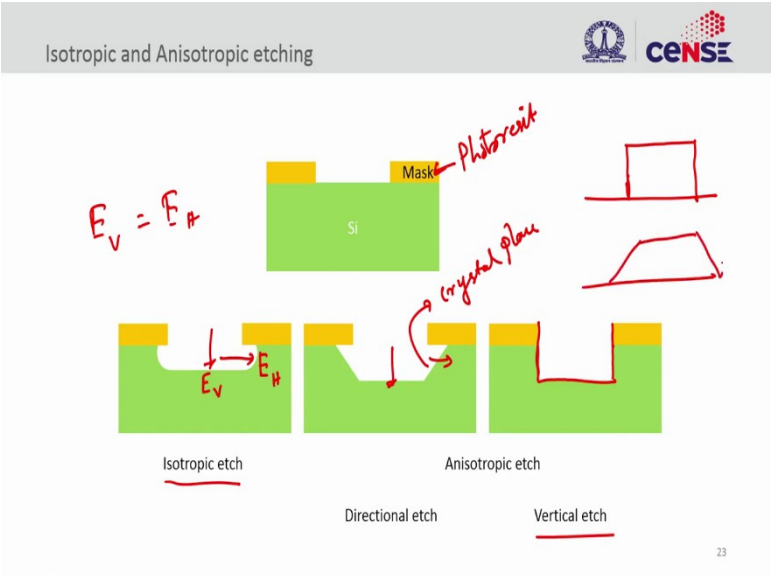

So, the dry etch process offers anisotropic etching, so we need to look at what do we mean by an anisotropic etching, so for that, I will use this cartoon where we have the photo mask here, this is photoresist and this photoresist is patterned using lithography now, so when we say isotropic, so the etching both in vertical direction and etching in horizontal direction are identical, so etch rate in vertical and etch rate horizontal, this is all equal, the removal rate in both the directions are identical, so that is called isotropic etch.

So, we also have something called anisotropic, so this is opposite of isotropic, anisotropy means there is some directionality, so that directionality could be based on the crystal plane or it could be just vertical, so this is physical etch where you just transfer the structure that we have, so you follow through the profile and then remove the material underneath, but in this case the direct, the etch is directional so there is difference in the etch rate vertical and horizontal.

So, this is also termed as anisotropic etch but more precisely this is called directional etch, so if you want to have your waveguide, you prefer to have it vertical, so in order to fabricate this it is better to use a vertical etch process than a directional etch process that will give you sloped sidewalls, which is something that we do not want.

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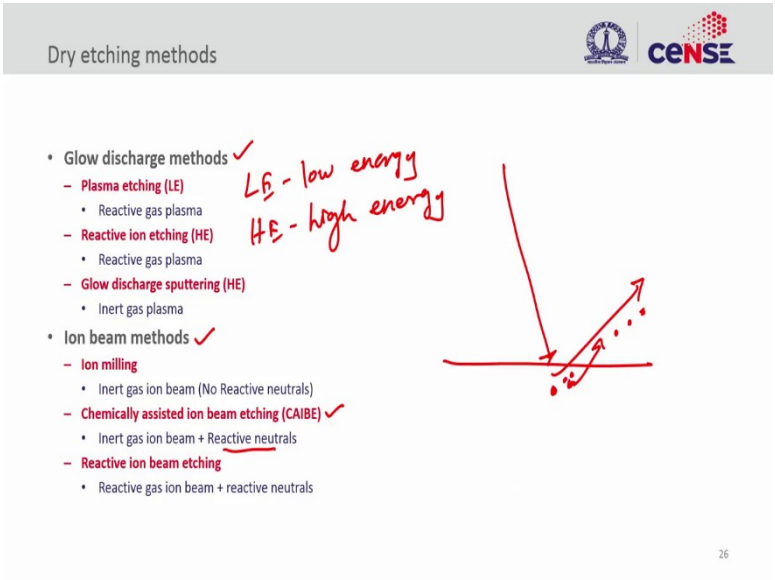

So, let us look at the different methods available for us to do this dry etch process. So, the dry etch process can be done with two ways, one is glow discharge matter, the other one is ion beam method. So, in glow discharge method we use plasma etching, we create plasma is called reactive plasma gas or you could do reactive ion etching which has high energy, so here LE is low energy and HE is high energy, so glow discharge sputtering is again a dry etch process that we can use that has high energy.

The other methods are based on ions, so in this case this is all reactive gas species, in this case we are going to use ions, very heavy ions that can be accelerated and then you can do ion milling of the material that you have on the surface, so this is a physical process where you have high energy ions that is kicking out the material that is on the surface. So, the chemically assisted ion-beam etching is another type of process that you can use which uses ions, but it is also reactive in nature.

So, the reactive ion beam is, the ion beams that are coming in the ions themselves are reactive in nature. So, in this case there are inert ions in both the cases they are not going to be reacting they are just going to kick out the atoms sitting here based on the momentum that this incoming ion has. But then reactive ion beam is something that where you use reactive ions, the ions are reactive in nature, so when they come, they react with the material and then take the material out. So, these are all the two methods of dry etching available to us.

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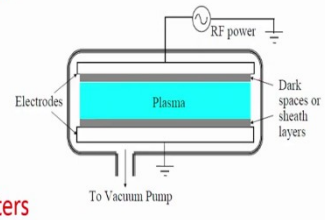
Complex parameter space

Plasma parameters

- Excitation frequency ✓
- Excitation power
- Gas flow rate
- Nature of discharge
- Geometrical factors
- Pumping speed



Plasma-Surface parameters

- Nature of the surface
- Surface geometry
- Surface temperature
- Surface potential

Complex parameter space

Plasma parameters

- Excitation frequency
- Excitation power
- Gas flow rate
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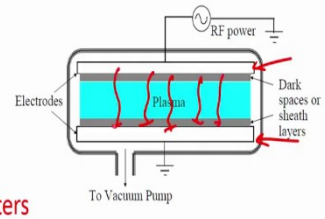

Plasma-Surface parameters

- Nature of the surface
- Surface geometry
- Surface temperature
- Surface potential

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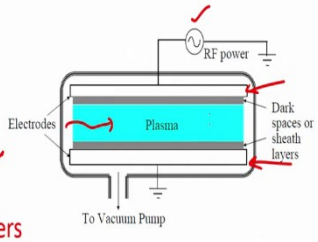
Complex parameter space

Plasma parameters

- Excitation frequency
- Excitation power
- Gas flow rate
- Nature of discharge
- Geometrical factors ✓
- Pumping speed



Plasma-Surface parameters

- Nature of the surface
- Surface geometry
- Surface temperature
- Surface potential

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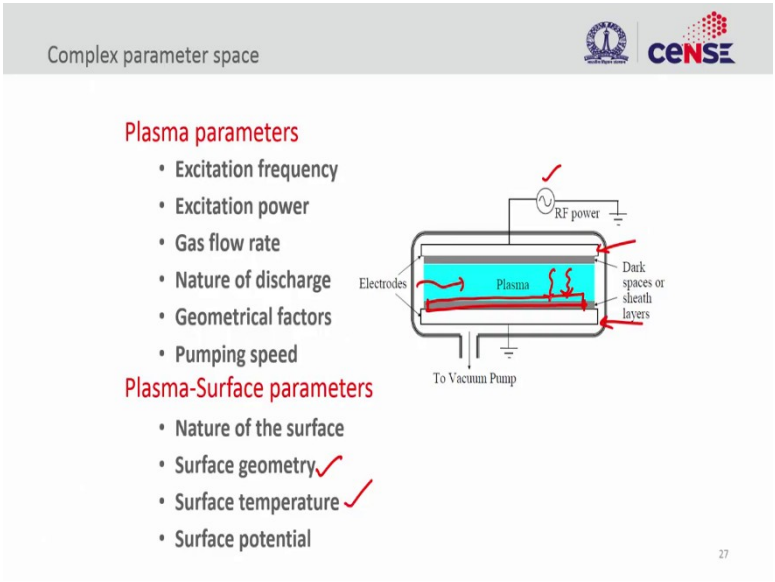

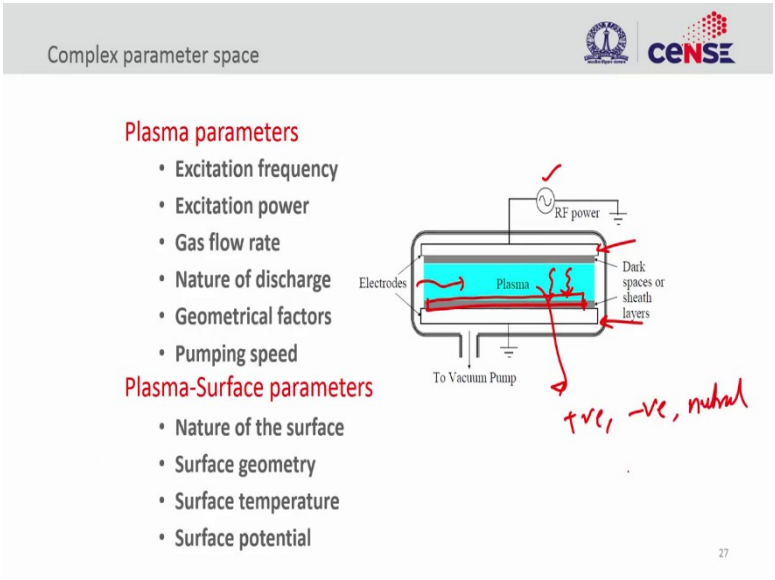

We primarily use the plasma process here which is a standard CMOS process and there are a lot of parameters to control the plasma, so you have excitation frequency into the plasma chamber that you have, so the plasma chamber, let me first explain how this plasma chamber is constructed, so you have two electrodes one is positive or negative electrode or you have the live electrode and the ground electrode and then this whole electrode configuration is put inside a vacuum chamber.

And then we apply RF voltage, so RF power into this top electrode that makes plasma between the two plates, so this is capacitively coupled plasma that is created here. So, there are various factors that determine the plasma here. So, one is the frequency that we have, the power of the RF, the gas flow because you need to create this plasma so you have to put some gas into this so gas flow, the nature of the discharge itself whether it is electro positive, negative, so normally it is electro positive in nature and what are all the gasses that you have there, the geometrical factor like how big or small the chamber is, the electrode is, and also the asymmetry between the electrodes, the electrodes need not be identical in size they could be difference in size.

And then the pumping speed, so the vacuum pump determines also the flow here and the pressure associated, so these are all the factors associated with the plasma and now the plasma is created but we are going to put the wafer here and expose the wafer to the plasma that is, that we created between these two plates. And the plasma to surface parameters are also important because that is what creates the reaction here.

So, the surface geometry is also important here that means whether it is the wafer is much smaller than the electrode or equal size the temperature you have on the surface here because the plasma species, the reactive species that are going to come onto the surface based on the surface temperature the diffusion length of this species are going to change. So, there are diffusion lengths associated with the etch, so your surface temperature should also be taken care.

And finally, the surface potential because you are, ions are going to be driven or the electrons in this case and also you have charged particles in this plasma that will be affected by the potential that you have on the surface. So, this plasma will have positive, negative and also neutral species, so you want to make sure that we take care of those species.

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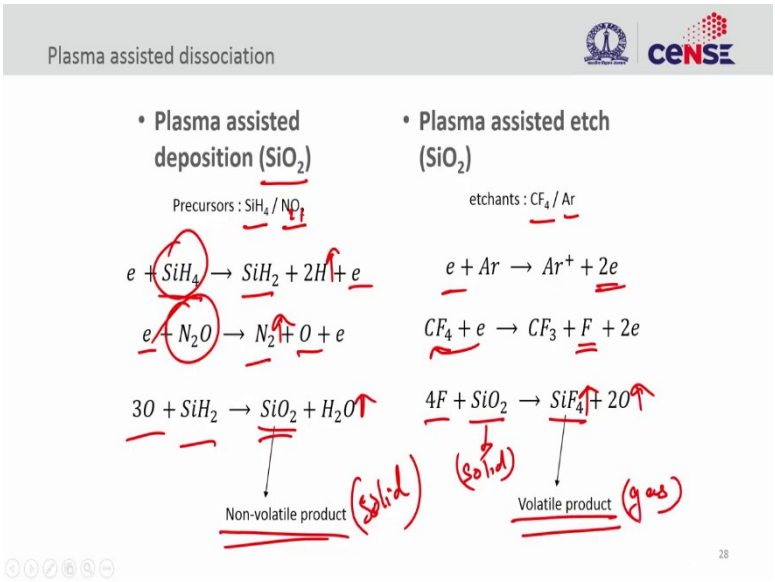

So, the plasma processes is not only used for etching process we can also use this plasma for deposition, we will see that deposition little later, so we can use the same plasma but using two different gases. So, for example if I want to deposit silicon dioxide, so this is a popular cladding material, there is a glass coating or amorphous silicon dioxide is a standard coating material that we do on top of the wave guides. So, that can be deposited by using silane gas and NO_2 gas.

So, the silane gas will be decomposed in the plasma to SiH_2 and 2H and a free electron here and then the electron will bombard with N_2O in this case creating N_2 and O, so in this case this is N_2O. So, here nitrogen is available and then the oxygen, so the nitrogen is a gas here and then the hydrogen is also gas. So, now we are going to make this oxygen react with this SiH_2 radical creating SiO_2 and then this water vapour, which is a gas again.

So, the whole idea here is you take two gases and then make them react with each other and create a non-volatile solid product. So, this is what we would like to do. So, we want to create a solid out of gas, so that is deposition, so we use plasma for that. And on the right side we

have etching, so now we want to etch silicon dioxide left side, so here we can do this by using CF_4 and argon, you can even leave out argon you can just do it with CF_4, but argon plays an important role here.

So, argon supplies lot of electrons, so it will supply electrons here and by supplying electrons, so that electron bombards with CF_4 creating fluorine. So, when you have 4 fluorine reacts with SiO_2 it creates SiF_4 which is a volatile product, so this oxygen is volatile, and this is also volatile. So, while you are silicon is solid or silicon dioxide here is a solid. So, you create a volatile product from a solid product is called plasma etching or dry etching process in this case.

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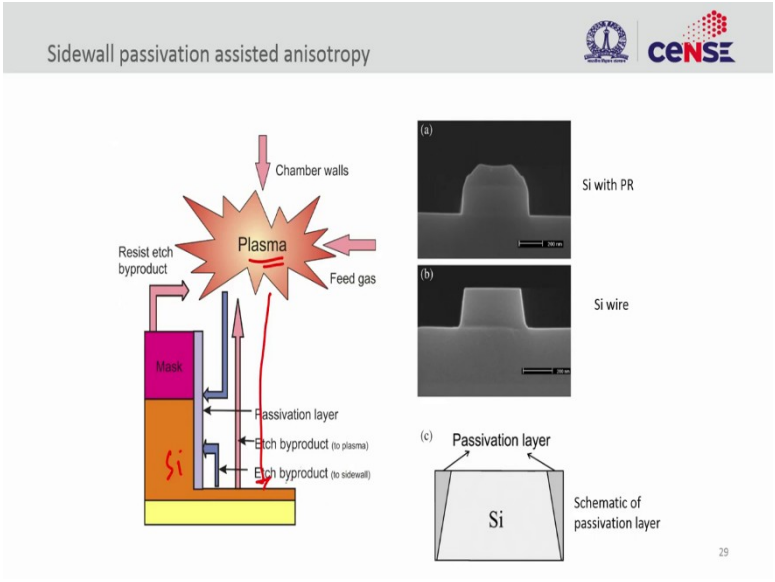

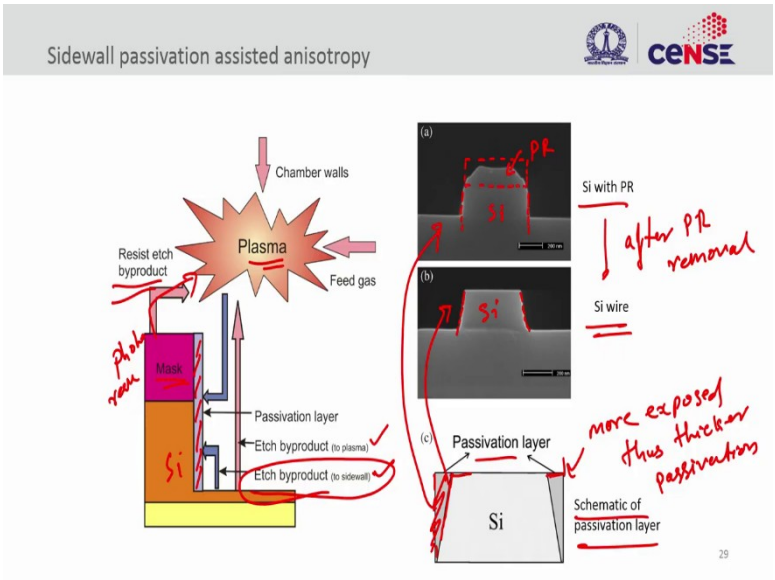

So, this is a cartoon that explain how this etching process happens. So, you have the plasma and then from the plasma you react with the material of choice in this case you have silicon, and it reacts with silicon and when it reacts with silicon it can create etch by-products and this by-products can go into the plasma or this by-products can go and stick onto this sidewalls. So, those two are possibilities or you can also have products from plasma deposited on the sidewalls also, with the photoresist that you have, this is photoresist.

So, the plasma will also attack photoresist and the products will go into the plasma again. So, what you see here is a silicon etch process, so this is silicon and what you see is here the boundary and this is your photoresist, you can see here it should have been like this but after etching silicon we have lost some photoresist because the plasma also etches photoresist. But then you can see here very vertical sidewalls, so the vertical sidewalls are here, but then after removal, after PR removal you see you get the silicon wire, so this is silicon.

But now you see a sloped sidewall, we do not have a vertical sidewall like we had here, so here we had vertical sidewall. But then when you look at this process more carefully, this vertical sidewall is just a illusion that illusion is because you have sidewall coating what we call the passivation coating and that is why I mentioned the by-products can also go and fall on the sidewalls.

So, when these by-products fall on the sidewalls they start accumulating because the top region is more exposed, so your thickness thus you have thicker passivation or the protection layer that you have, in order to create vertical etch. So, but when you remove this guy so this is what we saw here, so when we remove this, now the slope sidewall shows up, so when you are developing a etch process and if you want to have a vertical sidewall for your waveguides this is something that we should all keep in mind, you have to clean it up and check whether you are not seeing some illusion when you are doing process development.

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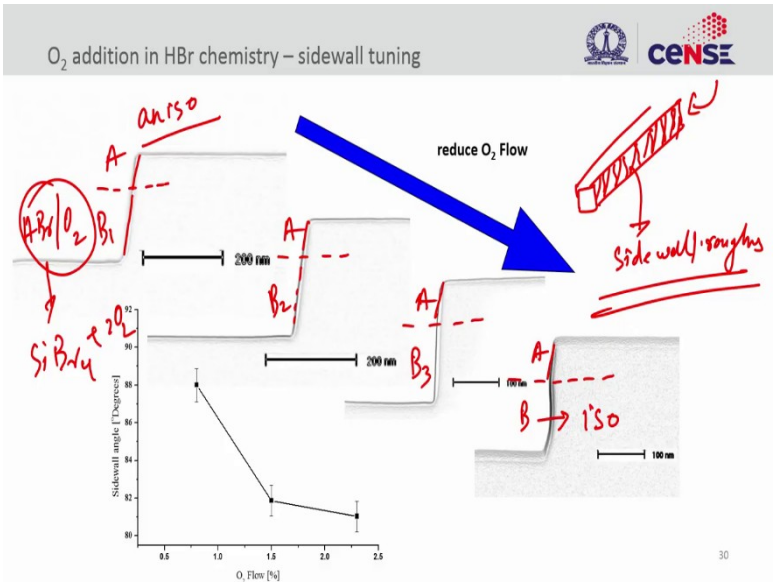

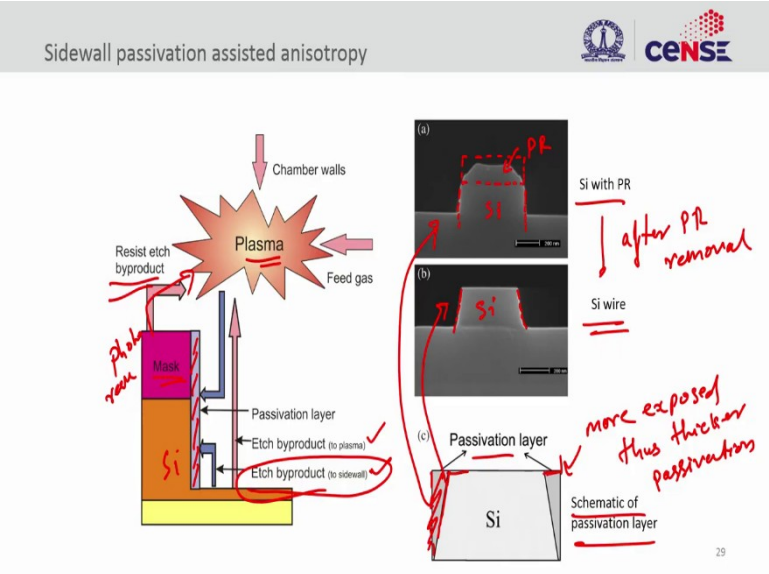

And the chemistry will also have a significant effect on the sidewalls. So, what is done here is a two-step process, so I am going to draw a dotted line where there is no change, so this is process A, A, A and A, so there is no change in that and that is the reason why you will see the same kind of slope along this, but then there is a change in the second process, there is B_1, B_2, B_3 and B_4.

So, in this process the HBr/O_2 chemistry is used to remove silicon. So, the silicon will be removed from this chemistry using $SiBr_4$ plus $2O_2$, so this is what will happen when you expose this to this precursor gas on to silicon. So, the oxygen plays an important role here as you can see when you reduce the oxygen flow you go from a sloped sidewall the positive slope to a negative slope, or in other words you go from anisotropic process aniso to iso process, because you are etching the sides here.

So, this is all because of our sidewall protection, you see here the sidewall protection that we had the by-product should go and protect the sidewalls, when you do not have sidewall protection the radicals would start attacking, so there will be etch from the sides. So, in order to protect that we use oxygen here to create that passivation, when you remove that oxygen, you will have attack of this sidewall.

So, why are we very sensitive about this sidewall? That is because when you take a wave guide, when light is propagating through this waveguide it will see the sidewall roughness, so we will have sidewall roughness. And this sidewall roughness can be avoided by using a process that protects this sidewall, so that you do not have any bombardment of ions onto the sidewalls creating damage or creating roughness on the sidewalls.

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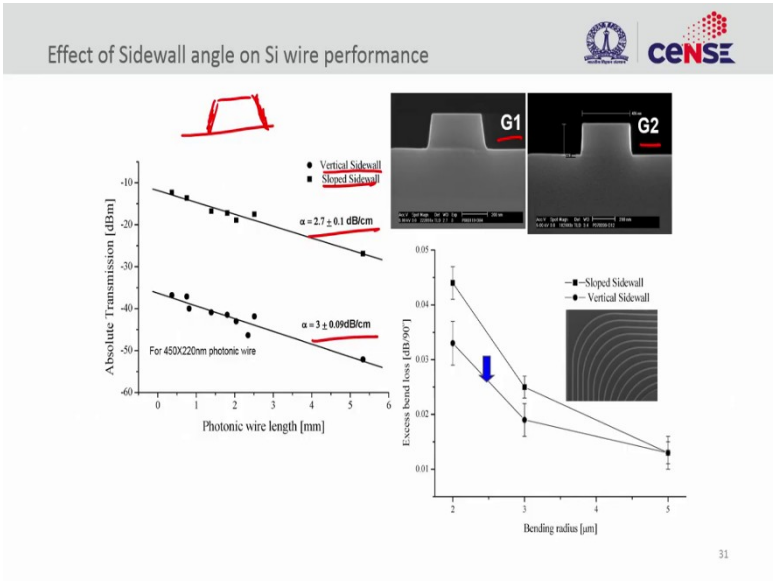

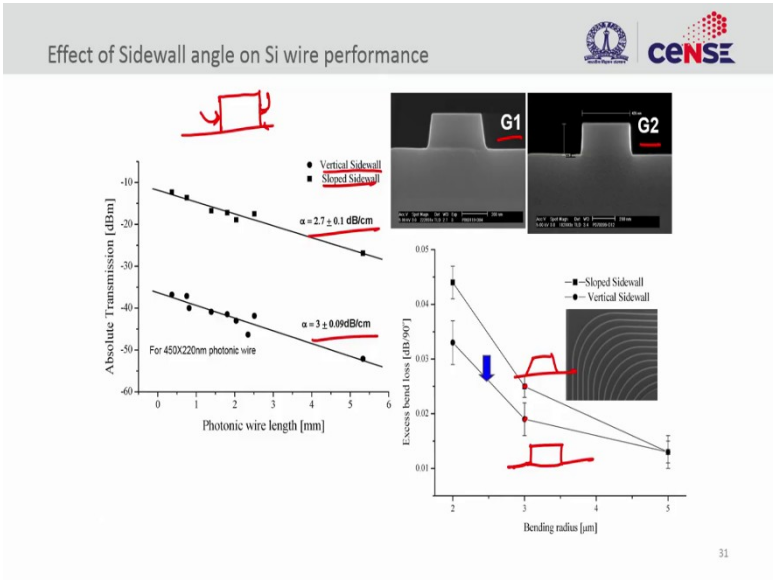

So, this is the effect of sidewall protection, there are two geometries we have the G_1 and G_2 where you have sloped sidewall and a straight sidewall. So, when you look at the vertical sidewall, the loss is about 3 dB per centimeter when you have a sloped sidewall, the loss is only 2.7 dB per centimeter. So, this tells you that though you have sloped sidewall, though you had a slightly sloped sidewall, the sidewall was protected from the ion bombardment.

And the sidewall roughness is low that is why you have lower loss for sloped sidewall. But for a vertical sidewall you expose the film completely without any protection and that has created lot of sidewall roughness. So, this is a good thing, when you using a waveguide with lower loss, so you can have slightly sloped sidewall. But there is a downside to it, the downside is polarization effects.

So, when you have waveguides with sloped sidewall you will have more bending loss coming from your polarization crosstalk, so that is what is shown in this particular plot where the sloped sidewall, so this is the sloped sidewall and this is our vertical sidewall, so what vertical sidewall the bending loss is very small, so as the sloped sidewall the bending loss is high, so this is the excess bending loss coming for this, this is a characteristic of a polarization, crosstalk or loss in the band itself. So, when you are building any circuit you

should make sure that the waveguides are not trapezoidal in nature that would result in this kind of propagation losses.

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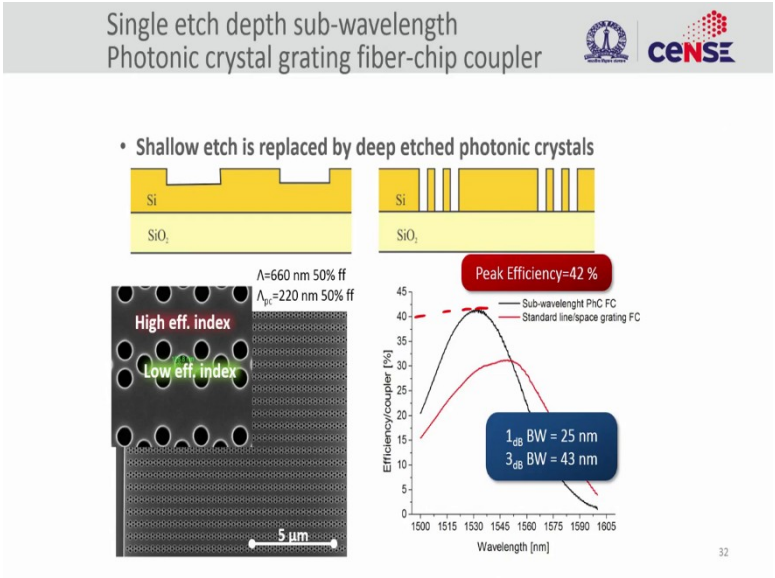

So, you can use this patterns to do even finer feature in this case, we can make a photonic crystal based grating couplers, these are very fine features you can make this deep etch structure and based on this you have really good coupling here, so this is coupling between fiber and photonic IC you have about 40% coupling efficiency if we use this photonic crystal based couplers.

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So, the next thing is about variability, so we looked at the fabrication of the structures by using dry etch process, so we used plasma in order to etch the silicon layer, but now you want to understand what is the implication of this etch on our device performance, so the device performance strongly depends on your etch process that we saw briefly, the etch process is going to create sidewall roughness and this sidewall roughness is going to scatter light, the scattering of light would result in loss.

So, we want to reduce that loss and that loss could be reduced by having a slope sidewall and the slope sidewall, not just slope sidewall the slope sidewall is a cause of sidewall protection, you create sidewall protection that would result in a sloped sidewalls not too much reasonable slope, but the slope sidewalls could result in polarization uncertainty and bending loss, so bend waveguides become lossy. So, we have patterned the structures now.

So, we looked at lithography, we looked at dry etching, but now we want to look at whether the devices that I make are going to be exactly of the dimension that I wanted. So, that is where variability of these devices comes in, so we want to look at whether this device are uniform or it is beyond, our control. So, let us look at that.

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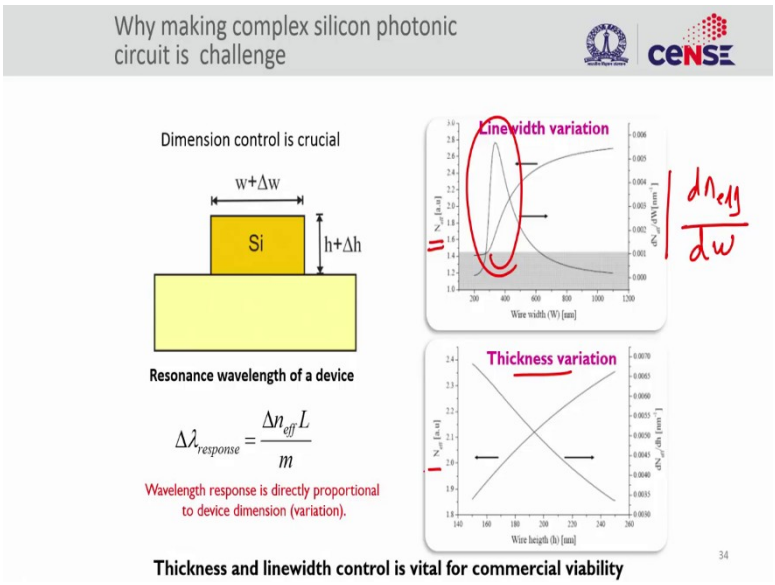

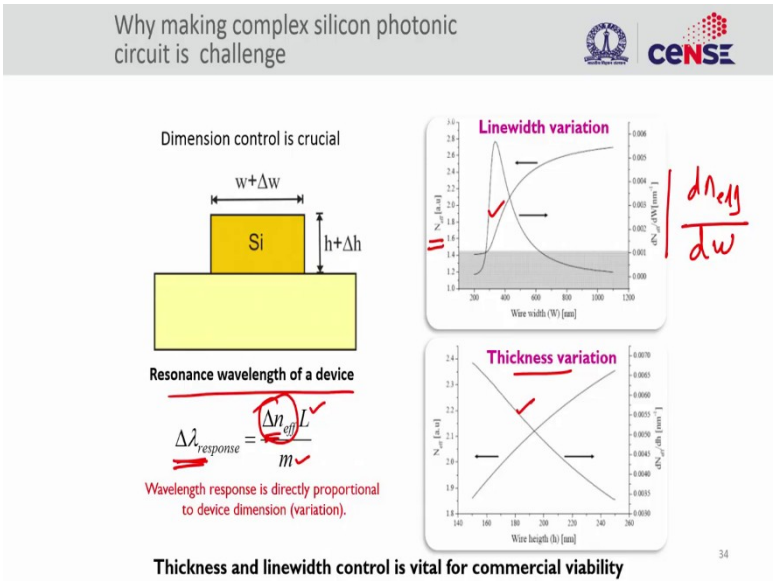

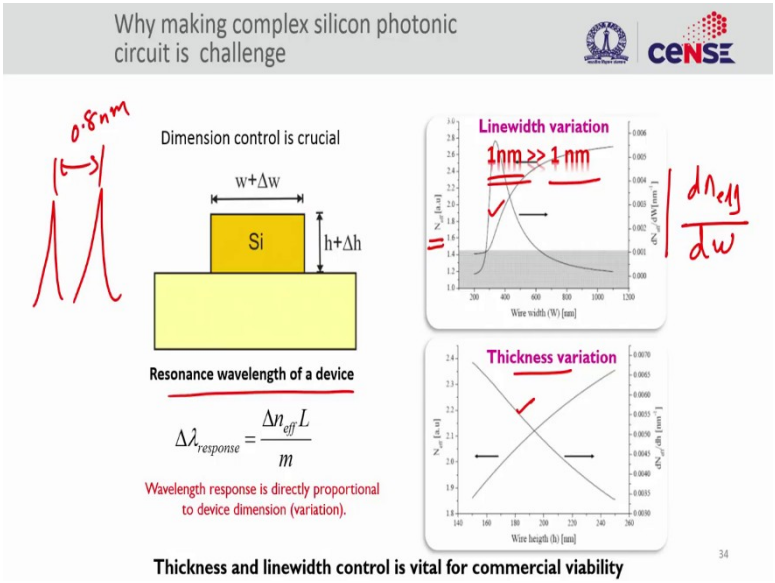

So, the device sensitivity can be easily calculated from the dispersion curves, so you have a wire waveguide here, so where you could look at the $n_{effective}$, so we looked at how to calculate this $n_{effective}$ waveguide design, so the $n_{effective}$ as a function of waveguide width. But the variability is nothing but dn you know $dn_{effective}/d_{width}$, you can see here when the waveguides are very narrow you see the structure is very sensitive to small changes in the width.

Similarly, when there is a thickness variation your effective index also changes. So, what is the implication if there is a small change in the width our $n_{effective}$ changes. So, what is wrong with this? The problem here is all our device response is related to effective refractive index, all the designs that we do even cavity lengths 2nd, so your refractive index is very important in this case the effective refractive index becomes very important.

So, for example if you take a resonant device like a ring resonator your resonance is directly proportional to change in the refractive index, so you are length remains same, your resonant mode, the resonant mode will remain the same, but when there is a change in the effective index because of either width change or thickness change your resonance wavelength will also change. So, it is important to make sure that your thickness and the line width is under control unless you have that cannot fabricate devices that are reproducible and also large volume fabrication compatible, so we want to make sure that you have reasonable uniformity.

And just to give you a number, one nanometer variation in your waveguide width will create more than one nanometer shift in your response, so that is very large when it comes to communication, so we are talking about if it is 0.8 nanometer that is the 100 gigahertz channel spacing between two resonances let us say if the two resonances are placed 0.8 nanometer apart your one nanometer is your change itself, so the uncertainty is already 1 nanometer, if that is the case, then it is simply impossible to fabricate these devices. So, it is not possible.

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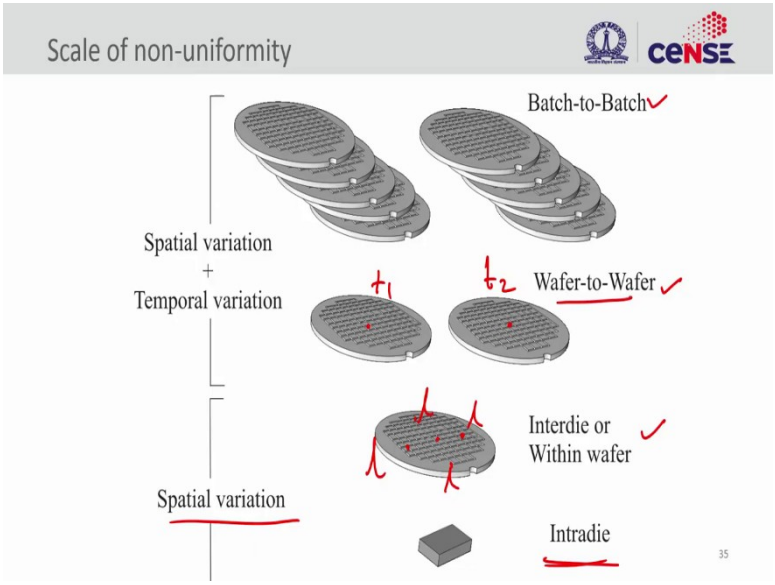

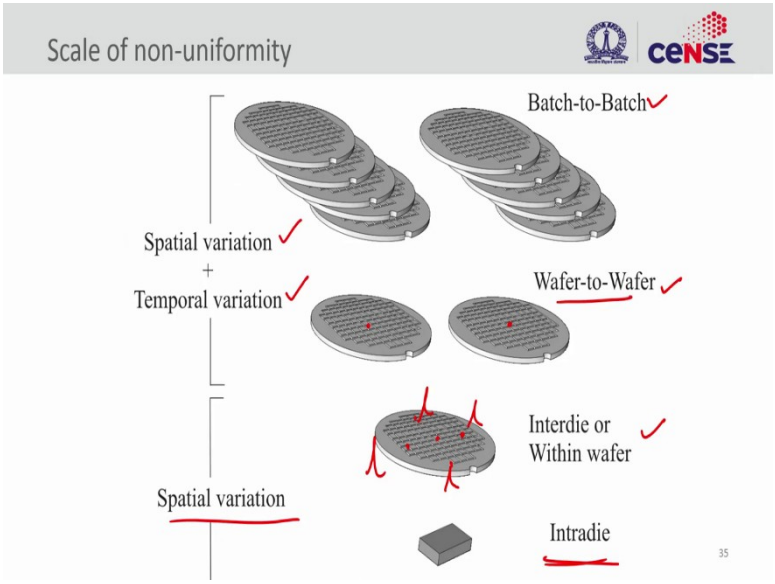

So, where is the variability coming from? So, variability can come from different places, so it can start from a single chip or the die, it can start intra or inter die or within the wafer or it can be from wafer to wafer, or it could be between batch to batch. So, this variation will be there, one should, one can control it, but you cannot completely avoid it. So, when you look at the intradie or even within the wafer variation it is primarily spatial variation.

So, the device difference between different locations, so how the response of a ring resonator here, here, here and here, vary, so this is primarily special variation. But then if you go for wafer to wafer, because this the device is, one wafer to the other wafer, so you process this at time t1, and this is processed at time t2.

Similarly, large volume batches will be also processed at different point of time, so as a function of time you could also have variations the process could drift because of time. And the variation now when you go for large scale is a combination of spatial and temporal. So, both spatial variation and also temporal as a function of time is going to be a problem here.

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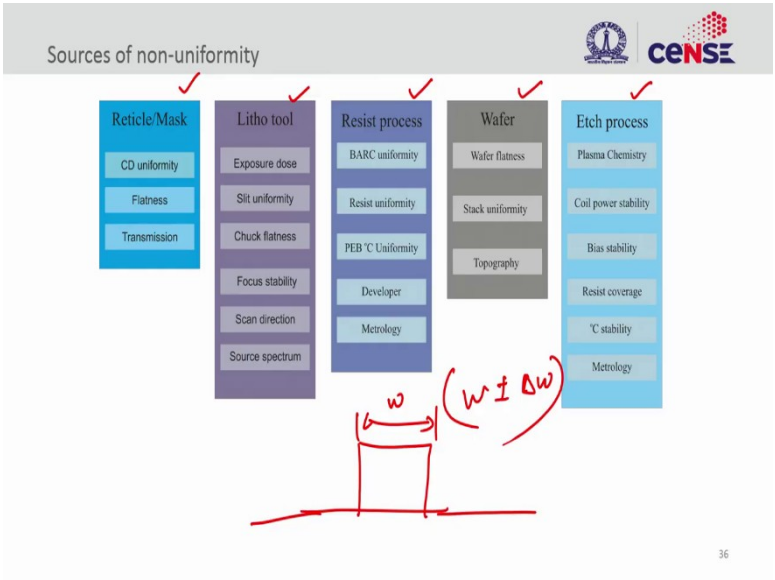

So, there are various source of this non-uniformity, where is this coming from? I know you probably are thinking that it is too much I think there is a, there is no way I am going to control this variability. To a certain extent the answer to that is yes, it is simply impossible to control your, [or] completely avoid variability, but you can control and keep it within a certain limit, that is what we try to do.

So, when you want a waveguide, so you have a certain width defined, so you ideally you want this to be w, but then you have to give some tolerance, so it can be plus or minus 10 nanometer, plus or minus 20 nanometers is what you are looking for. So, when you have this variation tolerance given then accordingly, we can choose and control the process here. So, it can come from the mask as I mentioned earlier, this can come from the lithography process, the resist process or the wafer in itself, the flatness of wafer, thickness of the wafer and so on and it can also come from the etch process.

So, I want you to spend some time just pause and then look at each and every thing that can go wrong and under each unit process, so we can, we can talk about in detail, but we do not have time in this particular course there is another course on micro and nano fabrication where the details are covered in that. So, here we just appreciate the fact that there is a lot of contributing factors when it comes to non-uniformity.

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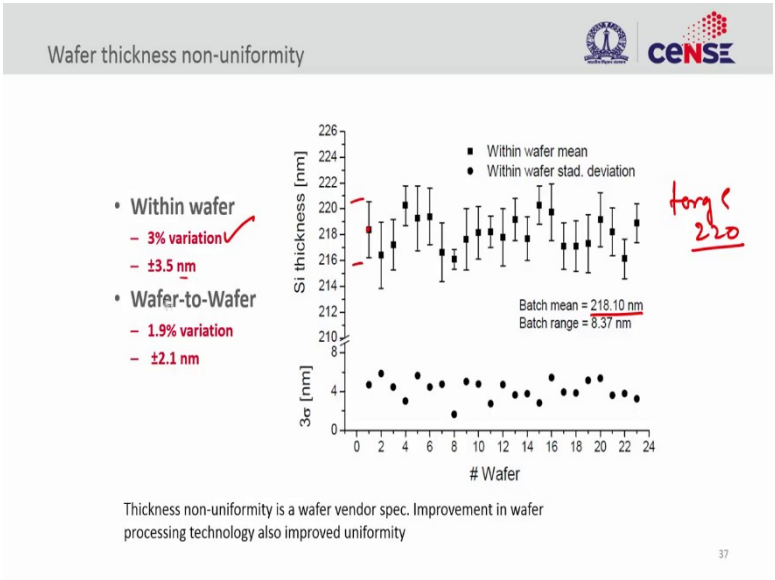

So, here we take a simple silicon, silicon on insulator wafer and then look at what is the thickness. The target is 220, but then your mean is only 218 and this is coming from each wafer, so there are 23 wafers here, so when you look at the wafers so there is a each wafer there is a variation, so within wafer we have about 3% variation that means plus or minus 3 and a half nanometers and wafer to wafer you have 2% variation, which is about 2 nanometer from wafer, to wafer. So, these variations are close to our requirement in terms of channel spacing or spectral response. So, one should take this into account when we are fabricating.

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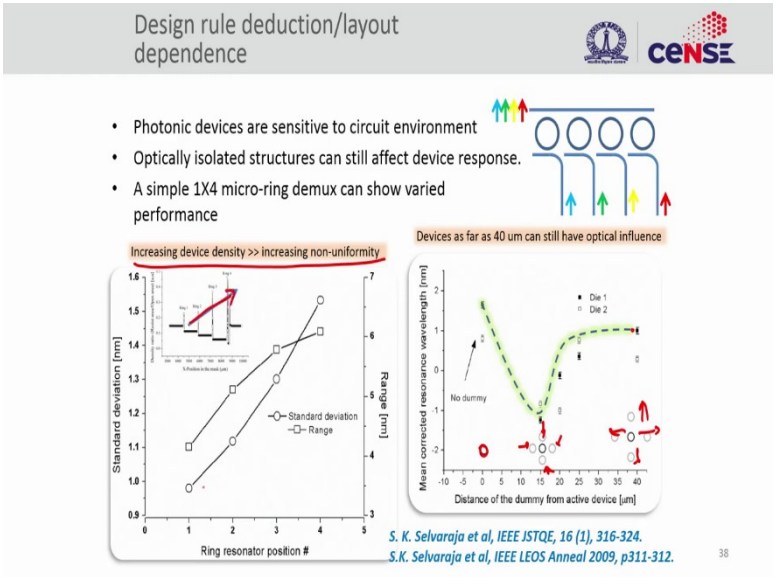

So, not only the thickness and the linewidth going to affect you, it is also the density of devices, so what do we have next to our devices will also affect your response. So, what you see here is a ring resonator and this resonator device is now surrounded by some structures, so here you have isolated ring, so this is a resonator, but then you have dummy structures or dense structure coming in.

So, when you have dense structures close to the device, then the response actually changes and then when they go out then you come back to the original response, so this is coming

from local device effects during fabrication. So, when you are fabricating this device the process for example the dry etch process strongly depends on the density of device.

So, your device density will affect your uniformity also, so when you want to cramp more number of devices make sure that you take care of the environment, so this is what is shown here, the density of the device is increasing, so is our standard deviation or the response itself is actually changing. So, one should be careful about the layout while you are designing this.

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So, once you have fabricated this device, we have to do the cladding.

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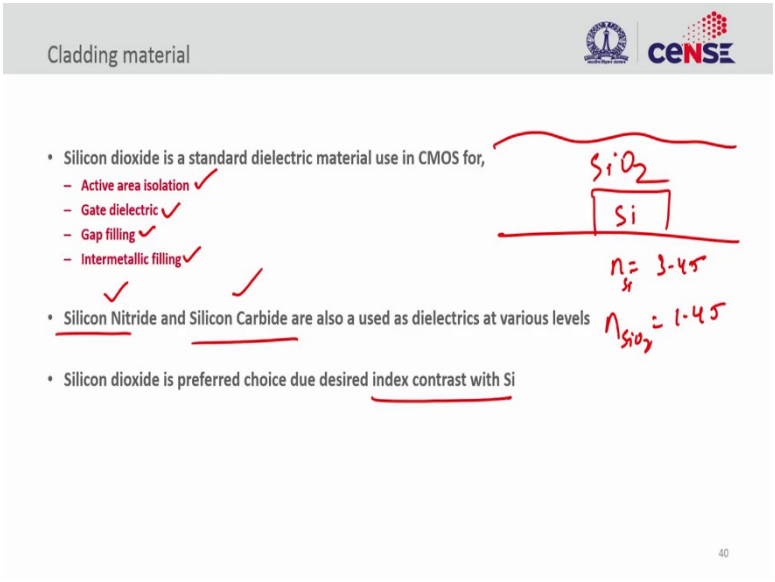

So, cladding is the cover that you put on top. So, in case of silicon or silicon nitride waveguides, so we put silicon dioxide as a coating material to protect the waveguides here. So, silicon dioxide as we all know is a standard dielectric material that we use in CMOS, so in microelectronics silicon dioxide is heavily used for various purpose that are listed here, you use it for active area isolation, gate dielectric we can use, we use for gap-filling and also intermetallic dielectric fill. So, intermetallic layer is also silicon dioxide.

So, at some point people also use silicon carbide and silicon nitride as dielectric in CMOS, but we use silicon nitride or also silicon carbide as a waveguide layer, if you like. So, silicon dioxide is preferred for all practical purpose because the refractive index of silicon is 3.45 and refractive index of silicon dioxide is 1.45, so you get good index contrast with silicon so we like to use silicon dioxide instead of any other dielectrics here.

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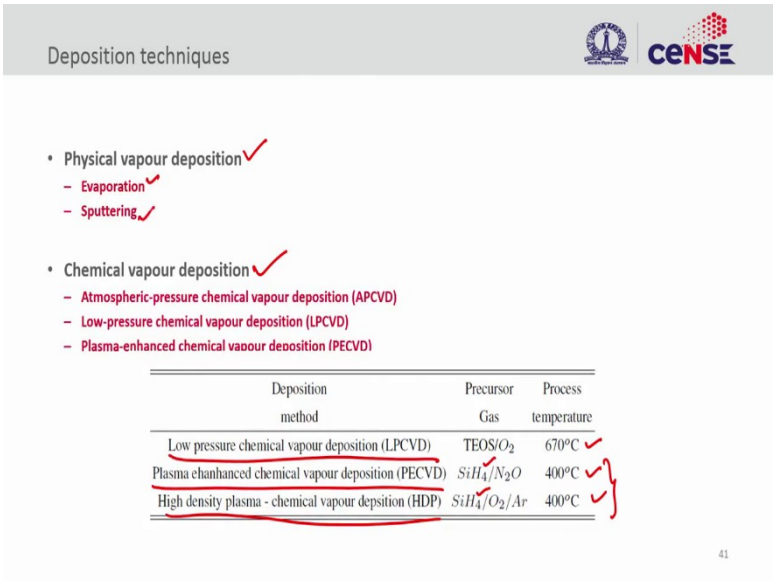

So, how do we deposit? So, there are multiple ways to deposit, we already saw plasma-based deposition, which is chemical vapour deposition, plasma enhanced chemical vapour deposition, we can also use low pressure chemical vapour deposition and also high density plasma deposition, so these are all different ways of depositing silicon dioxide by using different precursor gases primarily silane as a constituent gas, we can also do physical vapour deposition where we can physically transport the material which is good for certain application, but primarily for photonic application we want the material to be dense and uniform, so we use chemical vapour deposition.

As you can see based on this technique you can deposit at reasonably acceptable temperature 670 is really high temperature if you want to do the deposition on metals and so on you need to have low temperature process, so these are all the ways that you can do evaporation and sputtering in this case these are all the ways that you can deposit low pressure CVD, plasma enhanced CVD or atmospheric pressure CVD.

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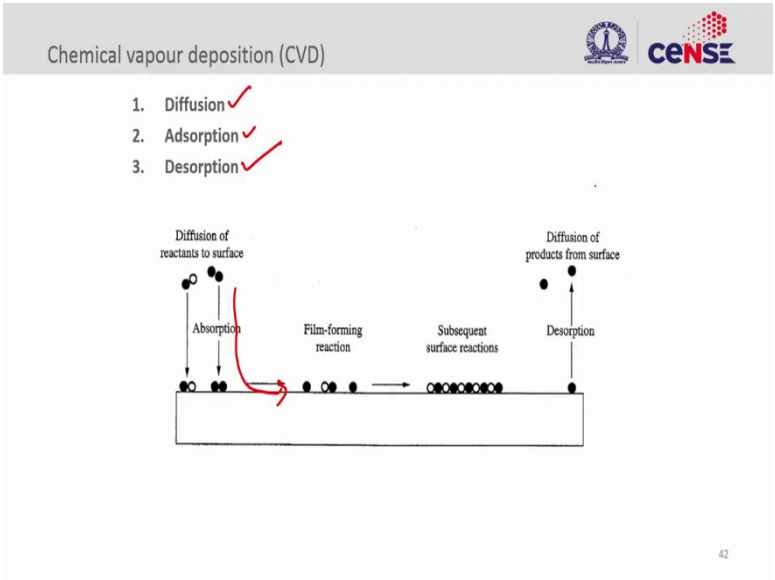

Your chemical vapour deposition process works reasonably straightforward the one process is starting with diffusion where the precursor gas diffuse onto the substrate that you have and then it gets adsorbed, so you get the product here that is adsorbed and then whatever reaction products that you have it will diffuse out, so desorbed out of this surface. So, whatever is adsorbed stays there, whatever is not adsorbed will leave the surface.

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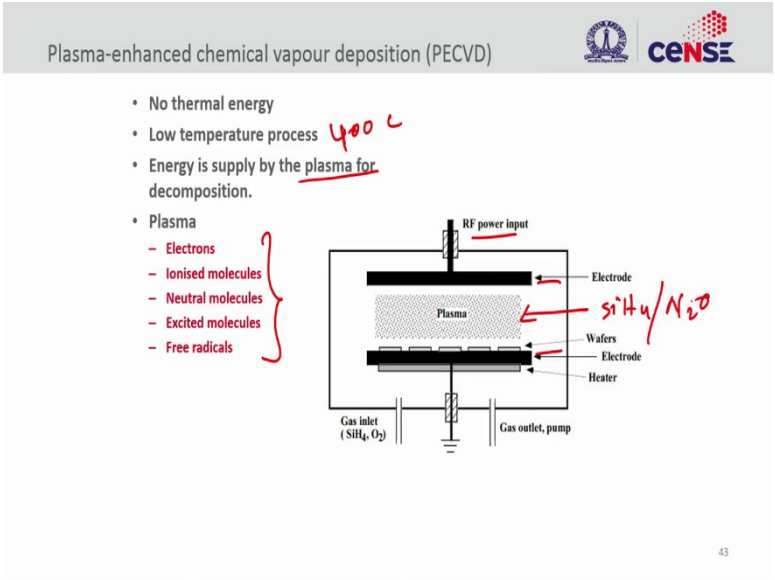

And this is again done using plasma process, there is no thermal energy provided this is done at 400 can do it at 400^0C relatively low temperature and the energy for this reaction is given by the plasma itself. So, this is something that we have already discussed earlier when we talked about etch, all the configuration remains the same, so you have RF, you have the plates here and the only thing is the gas here is SiH_4 and N_2O, instead of etch gases.

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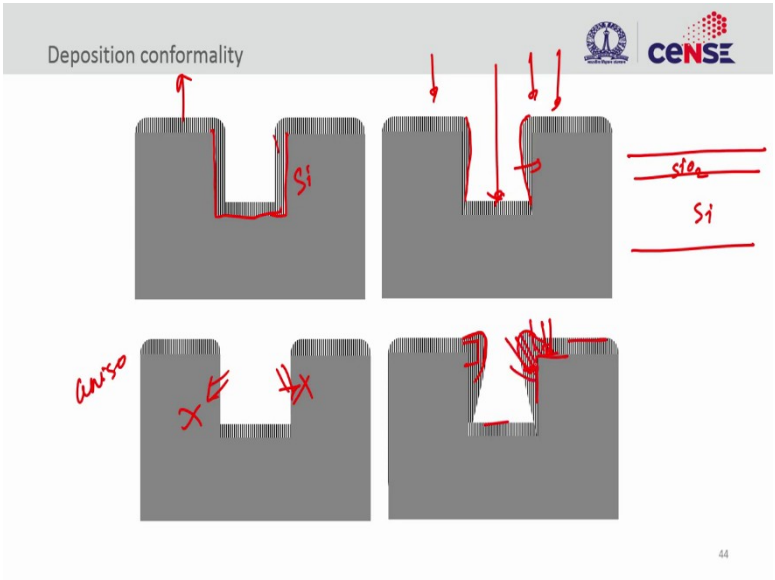

So, when it comes to filling, when it comes to depositing the material, so when you take a flat surface, it is relatively easy to deposit a uniform layer, but then when you have a topography mostly the case in our applications where we already defined a silicon waveguide, so now we have to fill this area.

So, if you want to fill this area, then you should make sure that you have a complete fill. So, this is a conformal filling, so this is what we call the conformal filling but then here you see a directional fill that has highly vertical direction fill where the sidewalls are not filled with the same amount of thickness.

And even more directional this is an isotropic fill there is no deposition on the sidewalls, there is completely no deposition on the sidewalls, so you could have another type of deposition where you will have something intermediary between completely isotropic and anisotropic, this could be an anisotropic process because of the angle that you have this collects more material compared to the flat surfaces here, because look at the angle here, you can get it from here and also, you can get it from here. So, you will grow much faster in these corners compared to flat surface.

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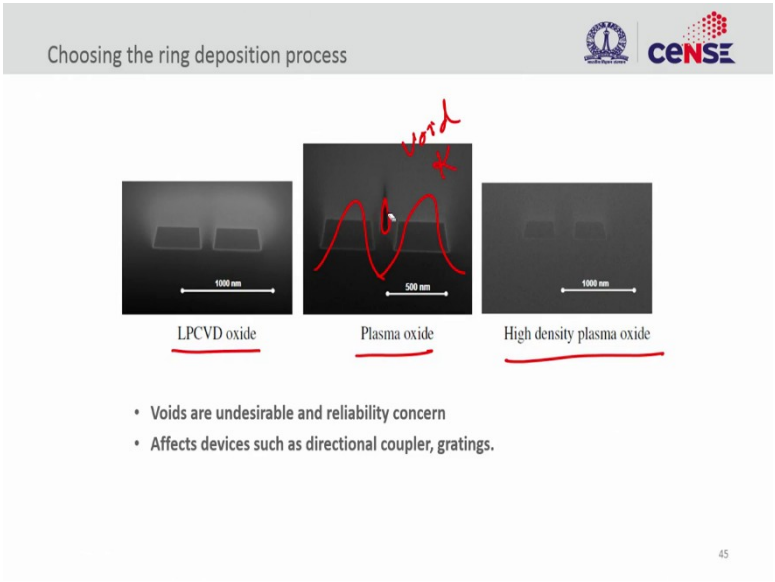

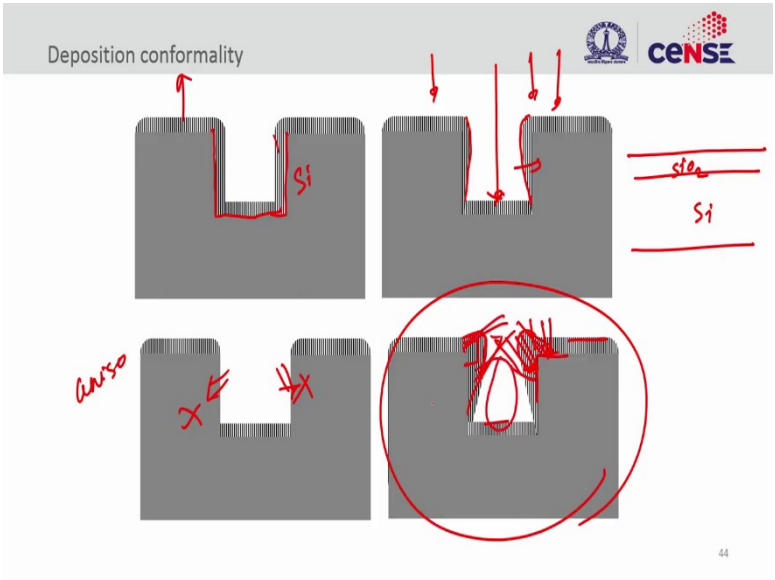

And this cross-section images actually tells you the SEM cross-section images tells you the different filling properties, you can see here LPCVD process, low pressure chemical vapour deposition process is a conformal process where you have smooth filling. And then we have high density plasma filling, which is also conformal, but then there is a plasma oxide deposition where you can see the void and this void is coming from our discussion about this.

So, these grow faster and then they will close creating a void here. And that is exactly what has happened here. So, when the material grows, it is depositing but it is depositing more creating what you call keyhole, a void here, so these voids are undesirable because of the reliability reason and also when you are having a directional coupler, so this is actually a directional coupler, the light is going to sit here but then the presence of void is to will change the κ between these two waveguides. So, any kind of fabrication non-idealities are going to affect your performance as this slide.

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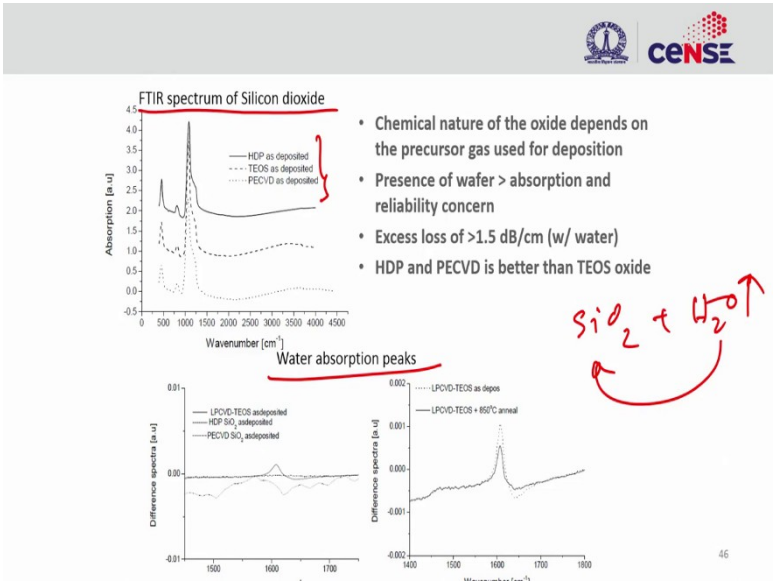

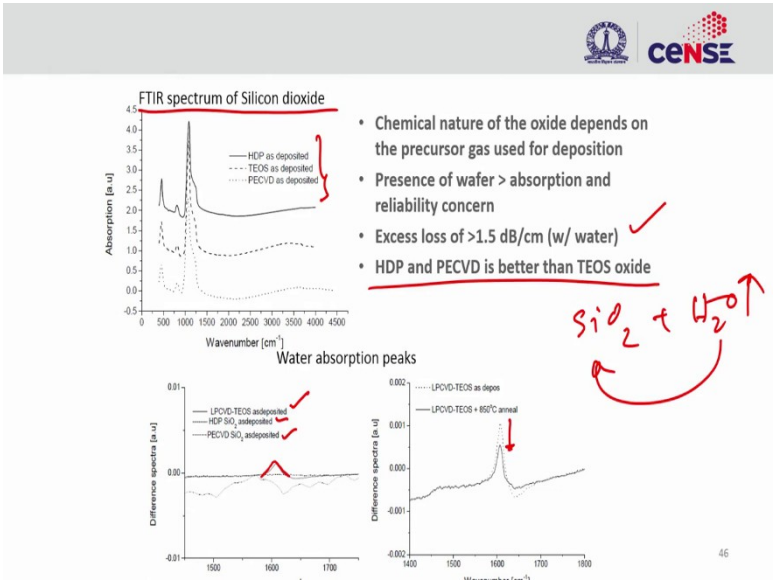

So, the next thing is about the chemical nature of the material that we are depositing, so this is a Fourier transform infrared spectrum of silicon dioxide, different kind of oxides, we talked about three different plasma oxide, so when you have these oxides, they also have absorption capacity to take water in.

So, there could be water absorption because the product contains water. If you remember our silicon dioxide formation results in water vapour, so this water vapour could be incorporated in silicon dioxide film and that would result in absorption particularly when you are working in IR range you will have absorption. So, how do we characterize that?

So, we characterize this by using FTIR, so you can see here for low pressure CVD technique using TEOS you see there is a water present here. And when you take a high density of silicon dioxide or PECVD process there is hardly any water present in, so we have to look at the chemistries that we do in order to make sure that we do not have any chemical absorbing species inside the cladding material or even waveguide material that you have.

So, one way of reducing is by annealing, as you can see here when you anneal the film you reduce your concentration here. So, material compositions are very important to understand and that should be done in order to assess whether there are some additional losses coming in

because of this material, so this is the very important material selection problem that you should look at, so the bottom line is using high density plasma or plasma enhanced CVD is much better than TEOS based or LPCVD, TEOS based LPCVD oxide.

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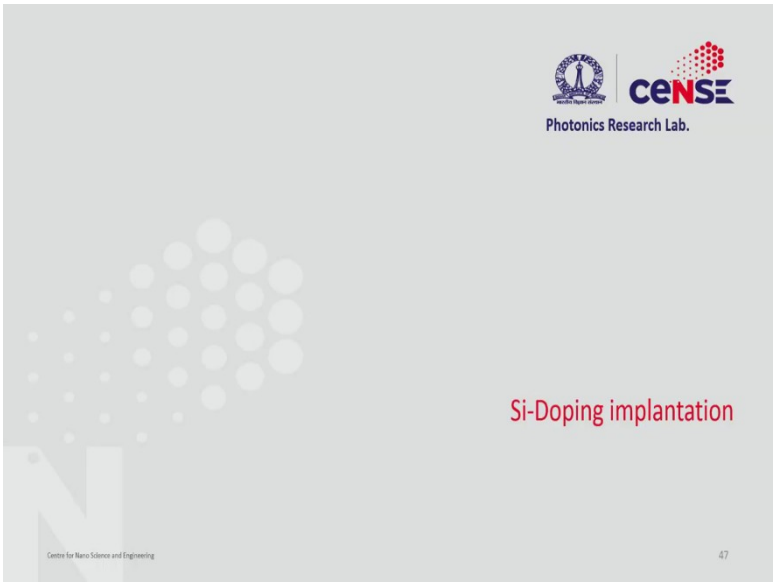

So, finally on the doping front, so we want to create let us say junctions.

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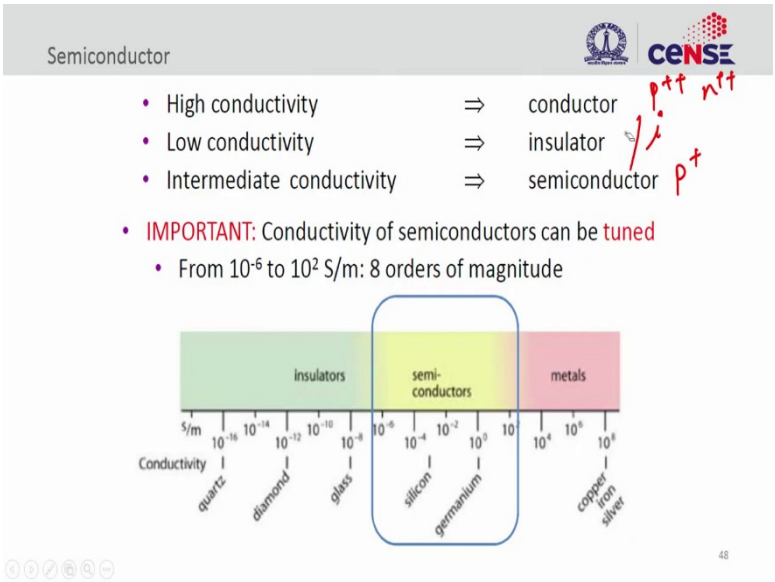

So, we talked about these junctions in our detectors, but we also use these junctions to create modulators in silicon which we will see shortly later. So, the doping is going to help you to change the conductivity that is the primary reason for creating this doped semi-conductors, so you could have high conductivity which is p or n++ so it could be completely insulating when you have really intrinsic material or you could have something intermediate where we could have p+ let us say. So, you could have completely intrinsic material like silicon dioxide that could act as a insulator, but silicon when it is completely undoped intrinsic silicon as a very very high resistivity, very low conductivity that we can also use.

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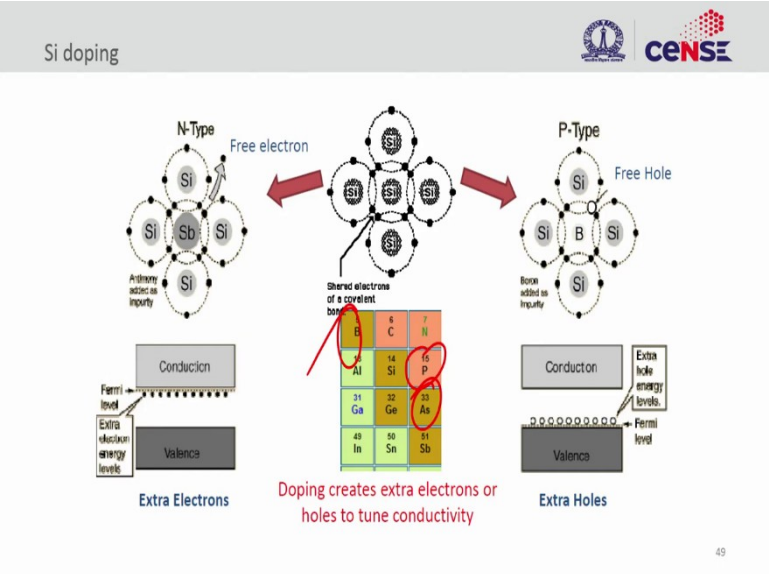

So, based on that we could dope this silicon by either using electron donor or electron acceptor and by doping it with in phosphorus or Arsene we can create electron rich species, you can do Boron doping in order to do p type, so or positive polarity here.

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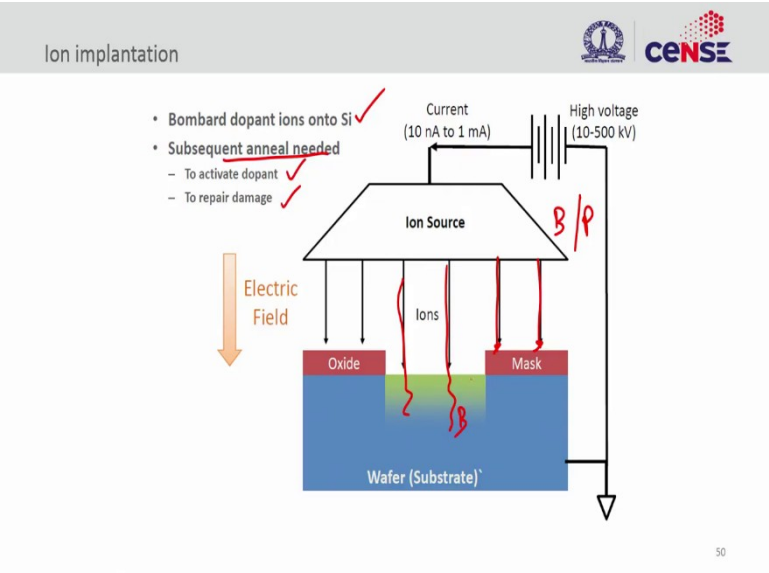

So, you can use any of this doping or dopants to create a doping, doped semiconductors that where you can create difference in the electrical conductivity. So, there are two ways to do it one is ion implantation that means you create these ions, so this is boron or phosphorus ions and then you accelerate it and these ions are accelerated and they bombard and then they are incorporated.

So, you have to bombard the atoms, the ions into the silicon and once you bombard it, they are just sitting there. But you have to make them react and that is what we call the activation anneal, so we have to heat it up that will result in activation and also repair the bombardment would create (())(43:17) amorphization of the silicon here, so when you are annealing it, it will recrystallize.

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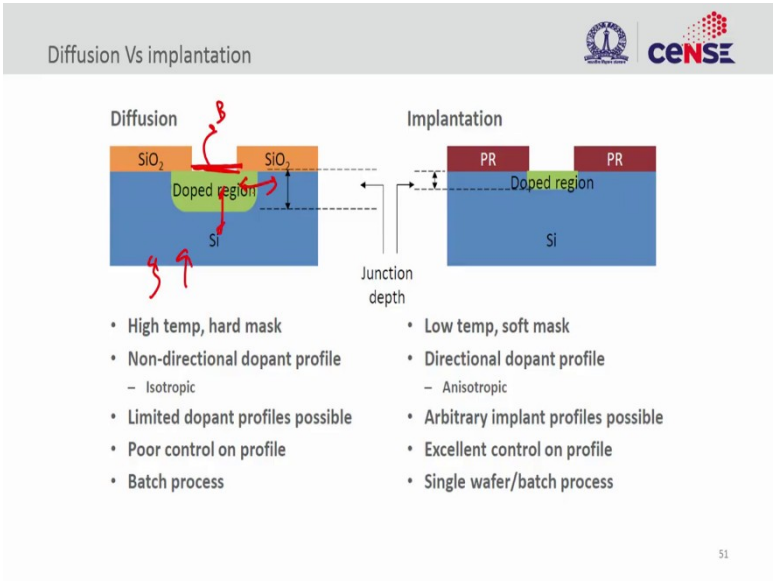

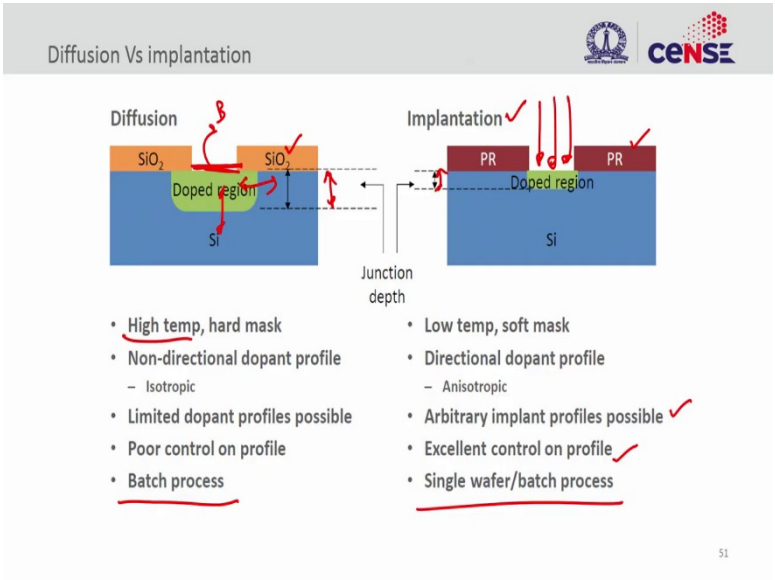

So, we can also do it by using diffusion doping, so in this case we can deposit a layer, oxide layer that contains Boron and then you heat it up, so the high temperature is used here, the only problem is this is isotropic in nature, so that the dopant will diffuse in all the direction equally, you do not want that and you can control that, so it creates profile control issues and we can do it with large wafers, so since it is a thermal process, we can put it into a furnace and then make this happen.

And you can see here the junction depth is very large, when you do diffusion doping because it is simply hard to control it. However, with implantation we can use photoresist mask here while you need to have silicon dioxide mask because you are using high temperature process. And here it is very directional because you are coming with some highly directional ions and you can create very shallow junctions, very sharp junctions we can make and we can have excellent control of profile and you can create any kind of doping profile, p, p++ and p or p p+ any kind of combination you can do it but the only thing is, it can do a single wafer process for large you can also do batch processing based on the size of your processing tool.

So, with that we come to an end of all the important fabrication process necessary to realize a simple silicon photonic integrated circuit. So, you can also apply this to other platforms like

silicon nitride or even polymer material and silicon carbide as well, so any type of process could be used to realize this photonic circuits on different kind of material system. So, for instance if we are going to use silicon nitride or polymer you cannot use this doping, for example.

So, only passive devices can be made, and those passive devices can be made by using deposition process to get the material and then using lithography and dry etching to pattern the material. So, these are all the fundamental processes that we will use in order to define photonic integrated circuits of your interest. Thank you very much for listening.