**Basic Tools of Microwave Engineering**

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**Lecture – 07**
**Lumped Element Based Impedance Matching Network Design by Smith Chart**

In the last lecture, we have seen the importance of impedance matching at microwave frequency. Now, in this lecture we will try to learn how to design an impedance matching network with lumped elements that we are familiar with lumped elements due to our low frequency network knowledge. So, up to certain frequencies typically up to 1 giga hertz lumped elements can be used for designing, but if we go at higher frequencies then these lumped elements their behaviour starts changing the same element, like a inductor if we go higher and higher in frequency and inductor also have some stray capacitances and other things.

So, that its behaviour may become less inductive sometimes even completely become capacitive etcetera like in our labs, if we do any experiment with a lumped element and try to change the frequency of the source that you excite this component to it you may see that sometimes it becomes capacitive, sometimes it becomes not at all resistive. Simply a resistor type of thing same with capacitor etcetera that is why at higher frequencies you cannot depend on these lumped elements that time you need distributed circuitry to have these f x of l and c etcetera. So, that we will see in the next lecture

So, this 1 is lumped element based impedance matching network design.

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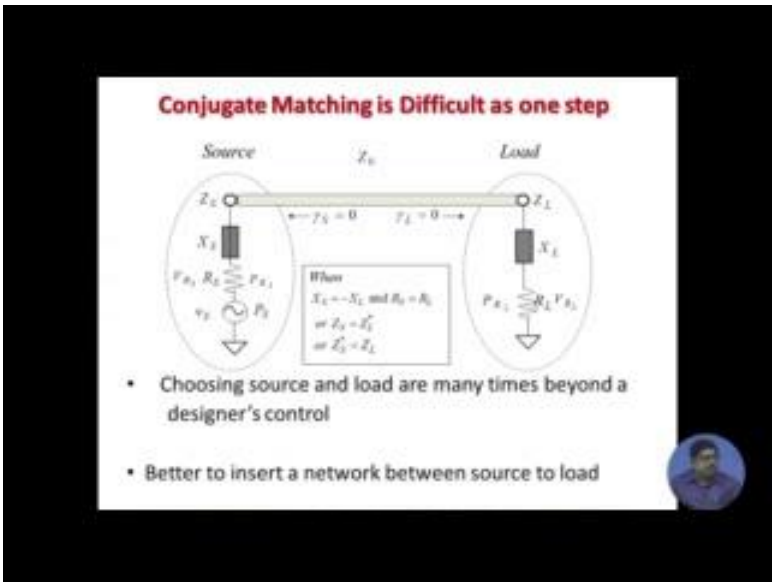


In many practical cases that conjugate matching, we have seen that it is ideal of impedance matching if you can do conjugate matching between source and load you can do many things. So, achieving both this gamma S that means, source reflection coefficient 0 and also the load reflection coefficient 0 by making the source and load impedance conjugate to each other, now that always is not at the hand of the designers.

So, a designer or microwave engineer he should be able to do that given a load and source, but always he can do put a network in between that is called impedance matching network and that network will do the job of impedance matching that we call impedance matching network. So, he should be able to insert a network between source to load for giving this thing, this is called impedance matching network.

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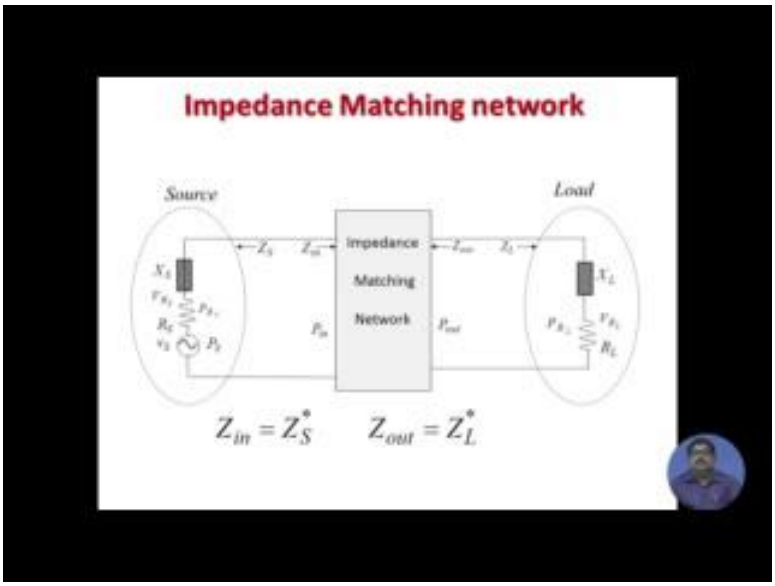


You see that in the impedance matching network. So, that there is an input impedance, similarly there is a output admittance of the impedance matching network. Now, these 2 he should try to conjugate match. So, that source impedance and input impedance Z they should be conjugately related also in the output side the load impedance and the output impedance, they should be conjugately related then between load and impedance matching network. You would not have any mismatch problem between source and the impedance matching network input, you would not have any mismatch problem. So, this impedance matching network design by lumped element we will now learn.

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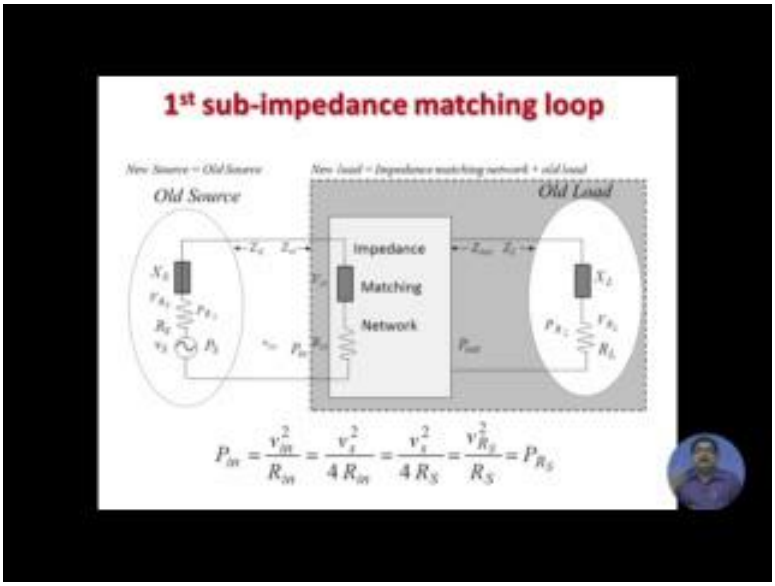

So, you see basically the whole thing, now has three sub impedance matching loops, the first sub thing is the old source is now replaced by the new source and the old source is looking at impedance matching network plus the old load network, the whole thing is now looking. So, what is the, but as we have already conjugately matched this source impedance and input impedance of this impedance matching network, there we can use that expression that P e will be.

Now, you can see that time we have derived in the previous lecture that in the conjugate match case the power that is delivered to the resistive part of a load impedance that is the V S square by 4 R l that time we said now here in the input side this first sub impedance matching loop that will give us P in is equal to V S square by 4 R in. So, you see that this is same as what power is having at the resistive part of the source the same power you can deliver at the input of the impedance matching network.

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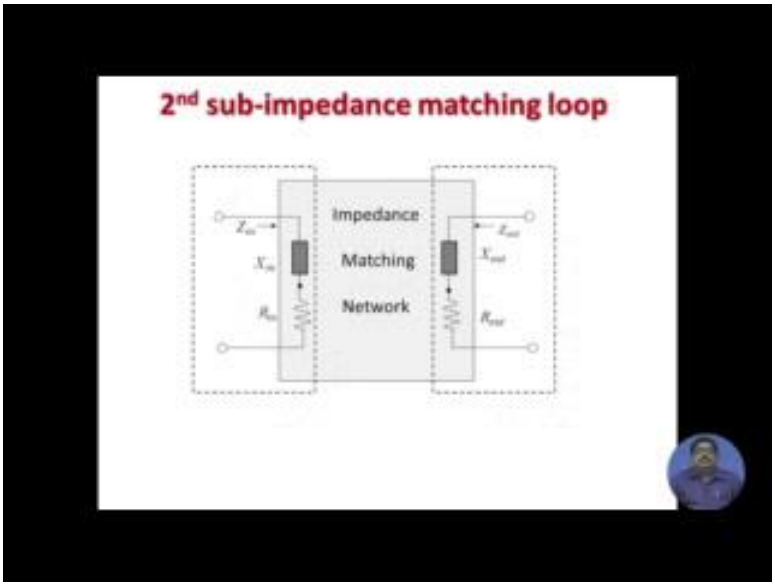


Then this is the second sub impedance matching loop as can be seen. Now, nothing special about it what happens to the third sub impedance matching loop the source side there.

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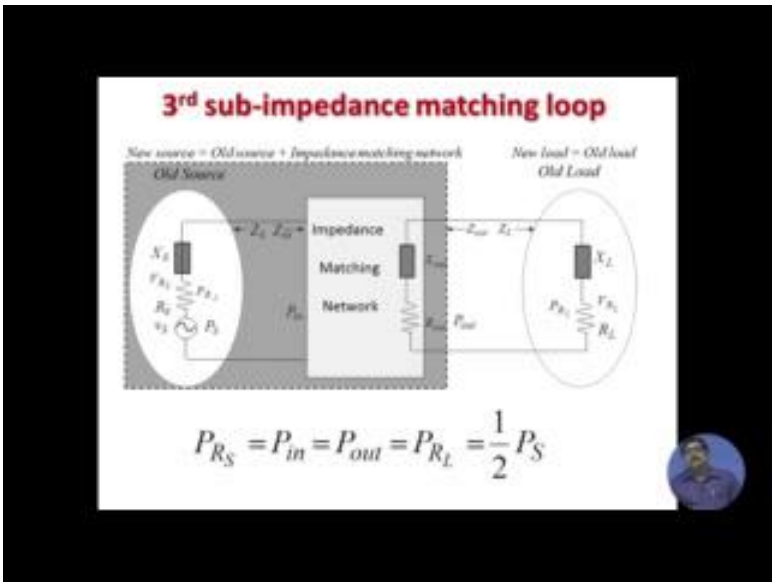


You can see that that P R S that has gone, as P in the first sub impedance matching loop now that power is again coming as P out and that is getting delivered at P l, P R l. So, the sources total power half of that is getting delivered to the load. So, this is the same case as the direct conjugate matching. So, with this introduction of impedance matching network also you are achieving the same thing that half of the source power source power is P S half of that is in the source resistance half of that is in the load resistance that thing you are achieving here.

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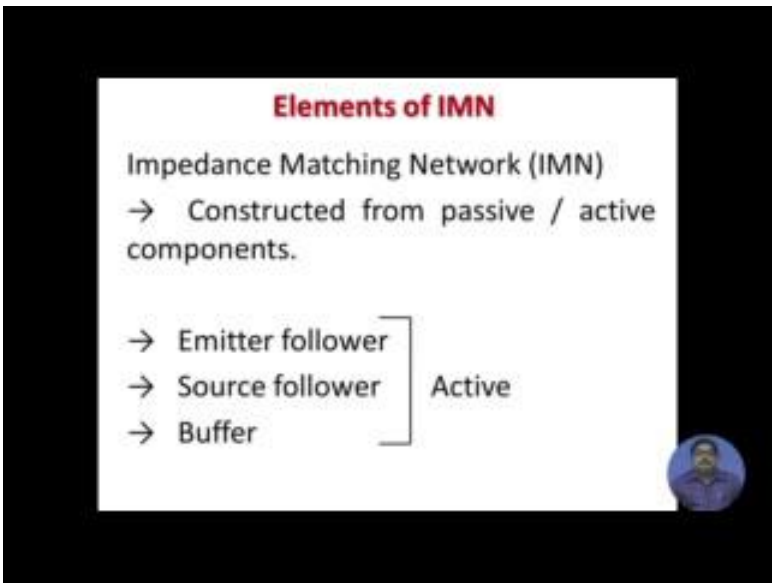

Now, this impedance matching network, IMN they can be constructed from either passive or active components. Now, there are good impedance matching network, they can be done with active elements like transistor based emitter follower source follower buffer there the active elements bits IFM.

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Now, problem with active IFM S is obviously, any active device it is having much more change of states electronic states and that is why the noise of the whole thing increases then any active device is much more costly than passive devices. So, cost is increasing; obviously, the any active device has a linearity limit that is why linearity also degrade and active devices many times have non-linearity's. So, you will have to be careful about that and current drain also increases in case of active devices because they have these active devices they draw lot of bass currents etcetera. So, that is why it is preferred that if you can if your purpose is served by doing the passive IMN, then that is advantageous.

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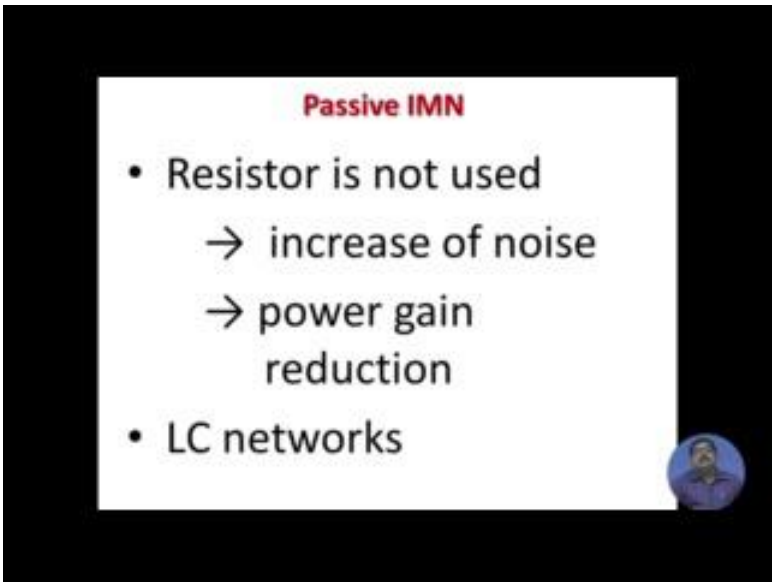


So, in passive IMN again you can make it with R l c, but resistor is generally not used again that it has some power dissipation. So, that is why if you can avoid, it is good also resistor again has a bit of noisy device. So, generally resistor is not used for passive integrated matching networks. So, mainly passive IMN by that we mean LC networks composed of either L or C.

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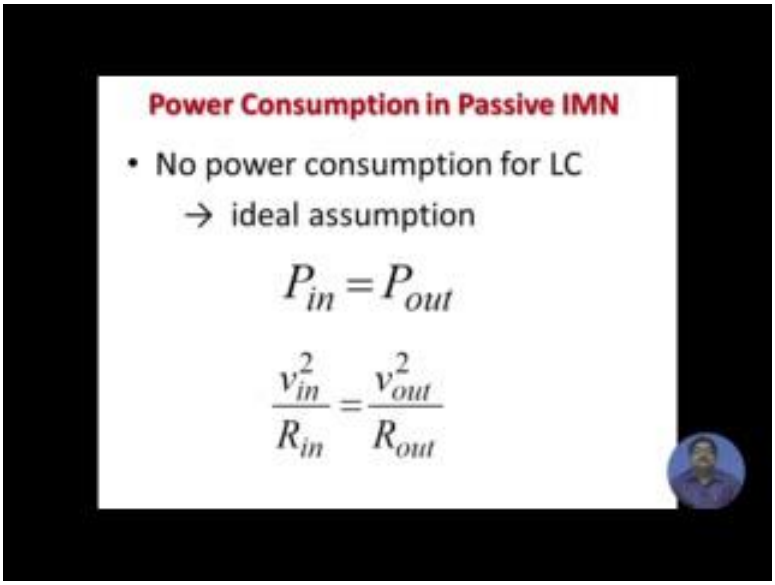


Now, if the L and C are ideal as I said that this assumption is up to a certain frequency after that frequency you cannot call them as ideal thing, but within that frequency range

that means, typically up to 1 giga hertz you can say that LC they are reactive elements. So, no power they dissipate in there. So, P in and P out are same for them that is why in the impedance matching network we get whatever you are giving as an input power to the impedance matching network if it is based on LC, this passive thing the same power you can take out there is no dissipation in the L and C.

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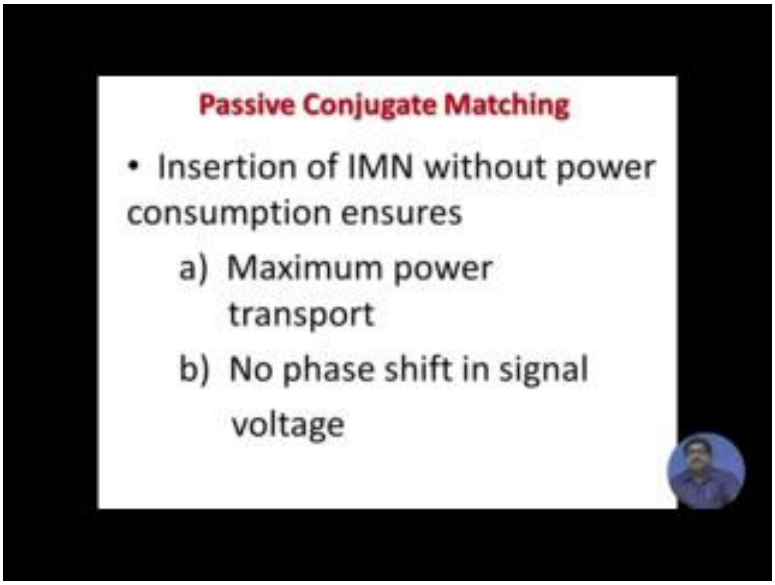


Now, you ensure the maximum power transport, no phase shift in signal voltage here also.

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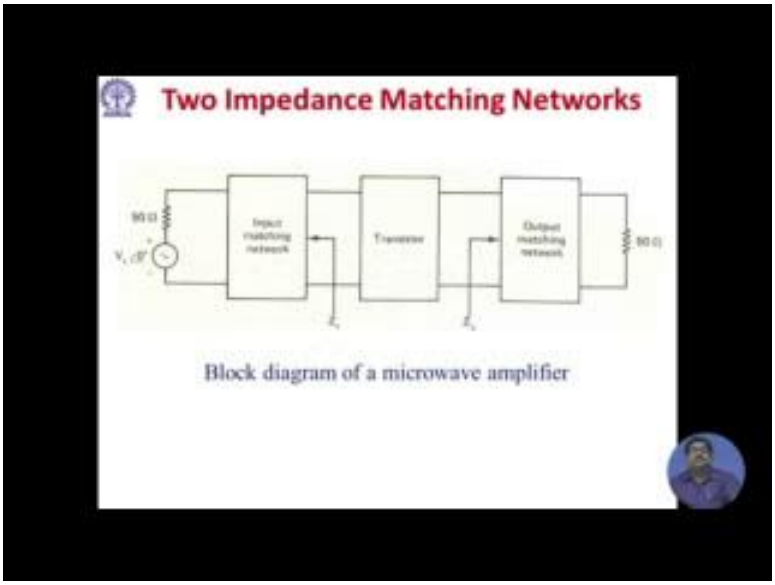

Now, generally if you want to have amplifier that time instead of 1 impedance matching network, you can also have 2 impedance matching network because of a transistor that in transistor, you know that it is a input and output there is a linkage between them that is why 1 single impedance matching network cannot always make the whole impedance matching there. So, because of the coupling between the input and output you know that either it is 3 terminal device any transistor.

So, which 1 you call input and output 1 of them is common. So, input and output there is a coupling that is why you need an extra level of matching network. Generally in any 2 matching network, but we would not talk of these in lectures. This is a designer of a microwave amplifier, he should know that how to do it is a mode involved touch.

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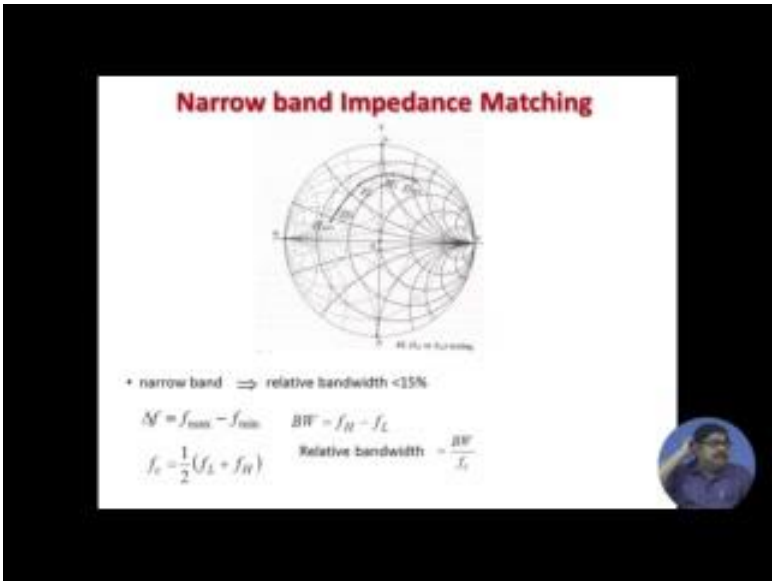


Now, basically we will see that if you are designing an impedance matching network, now LC base there what happens that L and C they are impedances, they are frequency dependant actually they have reactance which are frequency dependant. So, we can say the impedance of the matching network that is frequency dependant. So, it is at a particular frequency this match is achieved. Now, if you give a signal, generally you see any signal our base band signals that composes of various frequency signals. This is very reactive to get a single frequency like when I am speaking various sinusoidal signals are coming up.

So, it is a mixture of various nearby frequencies so that means, if an impedance matching network is matched at a particular frequency, but if the signal is a bit wider band containing bit wider band of frequencies, what will happen will the impedance match holds. So, you see that from this diagram that there is in the smith chart, if you plot the impedance, now if even with change in frequency the impedance does not change. It is rock solid at a point then it is a good impedance match, but as the curve shows that there is generally a variation of like that a locus of this as we vary the frequency.

Now, obviously that variation of impedance that should not be much because then the purpose will be lost, because we are trying to get particular impedance from this impedance matching network. So, that is why we define that what is narrow band matching? Narrow band impedance matching means the relative bandwidth which is nothing, but band width that is maximum frequency to which the network can be subjected minus the minimum. So, the bandwidth divided by the centre frequency that relative bandwidth is within 15 percent that is called narrow band design. At the end of this week lecture, we will see wide band impedance matching design where much wider band of frequencies that means, much wide signals which containing much wider band of frequencies, they also can be matched with that impedance matching network.

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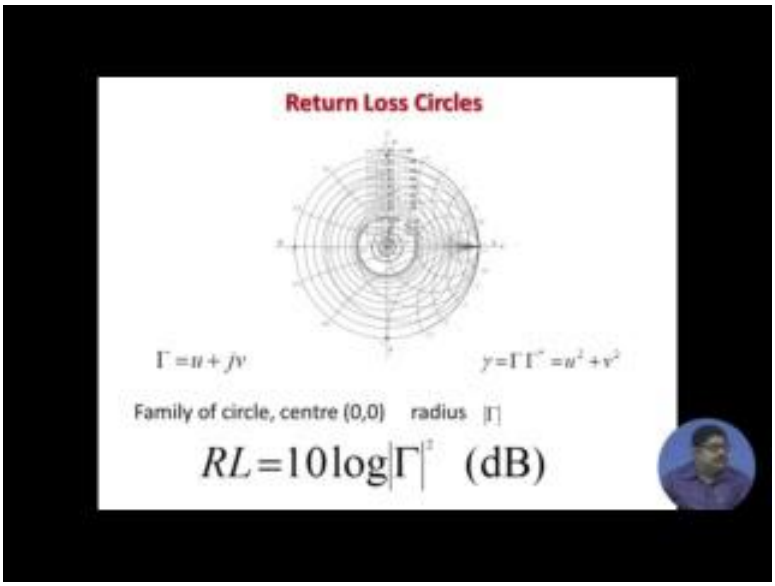


Now, 1 thing is you can plot that, suppose always the reflection coefficient even if you cannot make 0 you can make that. I will make return loss up to a certain level as we see

in the previous lectures that I have loss the reflection coefficient load reflection coefficient. So, power loss is this much that let us say tolerable in that case we can decide that what is the maximum load reflection coefficient you can suffer that means, return loss is defined as 10 log voltage reflection square magnitude square in dB scale.

So, we can plot it because if you have reflection coefficient that means, our in smith chart thing it is u plus j v. So, the power reflection coefficient that will be gamma is equal to this capital gamma into capital gamma star is equal to u square plus v square. So, in the smith chart thing now consider smith chart as a u v chart it is a reflection coefficient chart. So, u square plus v square will represent circles family of circles with centre at 0 and radius a radius given by the gamma magnitude. So, you can plot locus various circles of various or various return losses and see that whether that your impedance points they are within that circle.

If they are within that circle you know that return loss is manageable like in the previous 1 when you see that it is varying, now you can always see that, suppose I have also have a requirement that frequency may vary like this, but return loss should not vary more than this. So, if we this curve if we super impose on that return loss given circle from there you can see how much maximum return loss you can suffer and from that you can say that whether this design is or not. So, this is called return loss limitation

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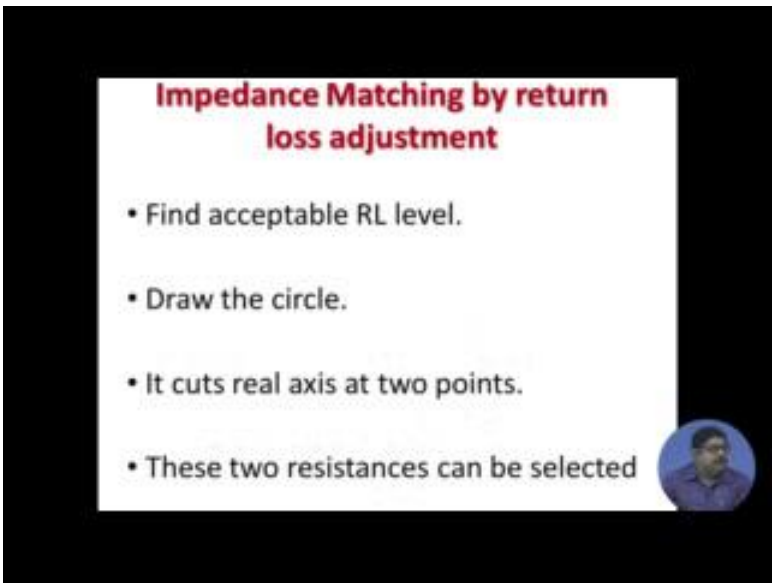

So, impedance matching by return loss adjustment, find acceptable R l level draw the circle it cuts real axis as 2 points. So, those 2 resistances at the extreme points beyond which you can need not go.

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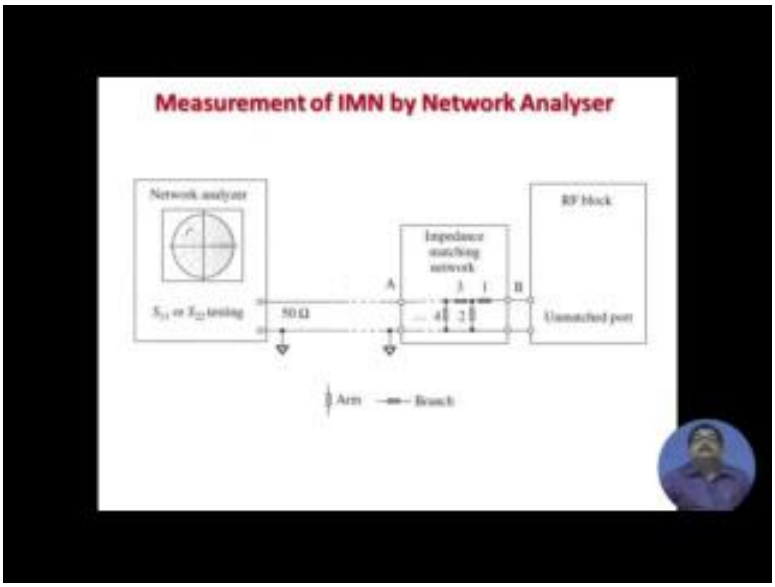


Now, this whole thing that how much is your return loss of any impedance matching network, you can use network analyser. We will study network analyser later in the this series of lecture. So, in network analyser you can connect the input port or output port of the impedance matching network and you can find various scattering parameters that also we will study later by that. You can find out that what is the behaviour of the impedance matching network? So, with the help of the network analyser you can study impedance matching network.

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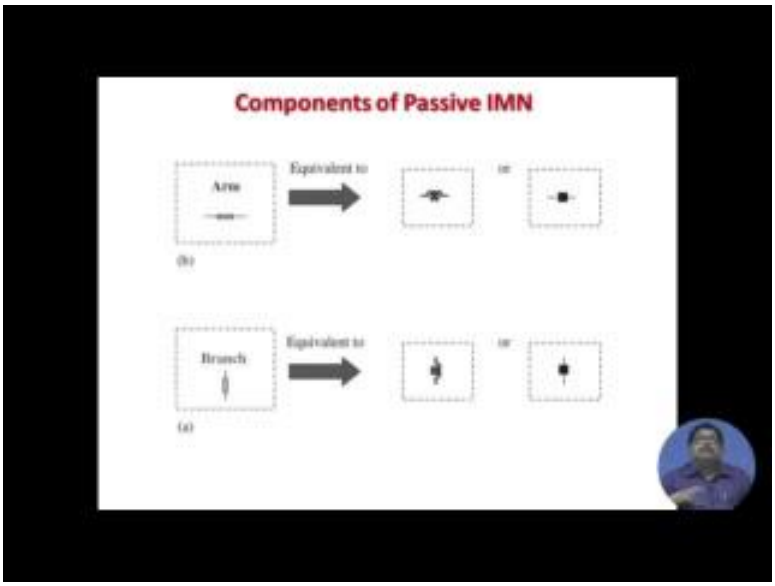


Now, let us come to the passive IMN design. So, there are various things in their terminology the 1 arm means generally a series element. So, it can be inductor or a capacitor. So, arm means series arm branch means a parallel branch. So, that also may be L and C, so that means, you can have either an inductor or a capacitor in series a inductor or capacitor in branch etcetera various combinations of that.

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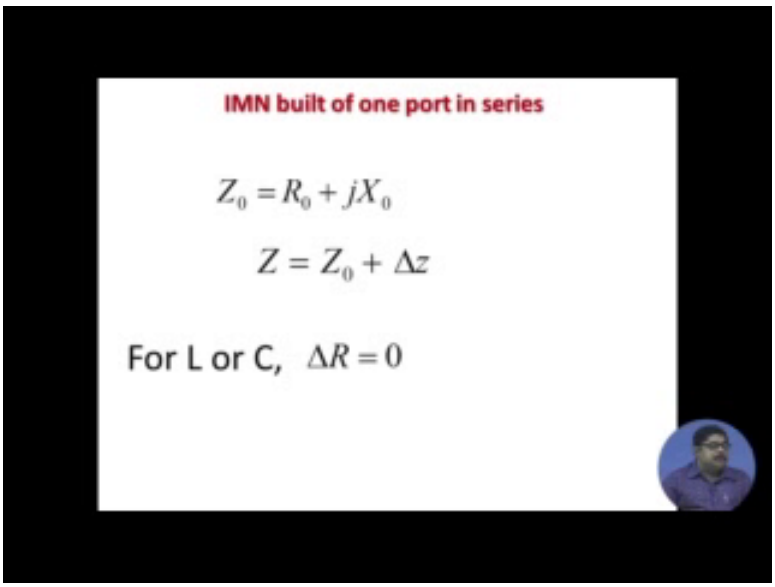


Now, let us say that IMN built of 1 part in series. So, in that case, suppose Z naught was the previous impedance with that you add 1 part. So, Z becomes the new wave, if it is in

series the extra delta Z is given by that extra arm. So, for L and C delta R is equal to 0. So, you are adding that delta Z.

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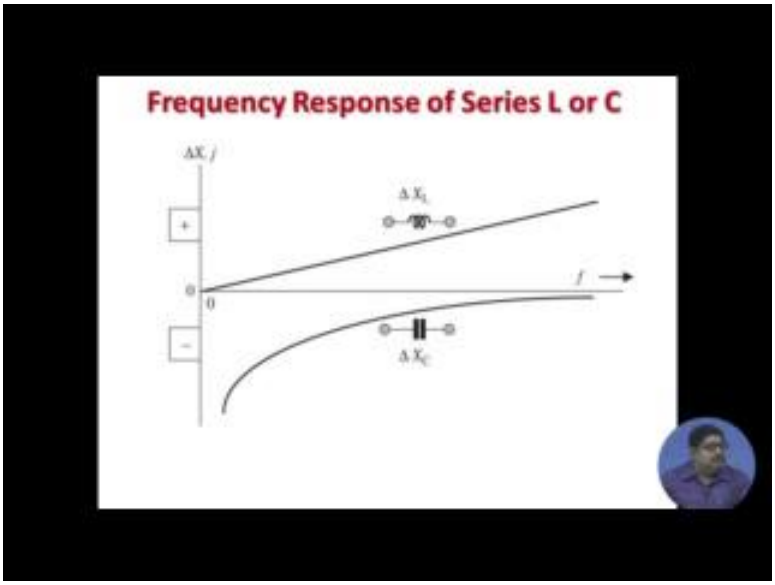


Now, frequency response of a series L or C you can see that that varies like this is the frequency response. So, for inductance it is linearly varying for capacitance it varies not inductly, it is a hyperbola type of variation and you know this this this frequency response is known.

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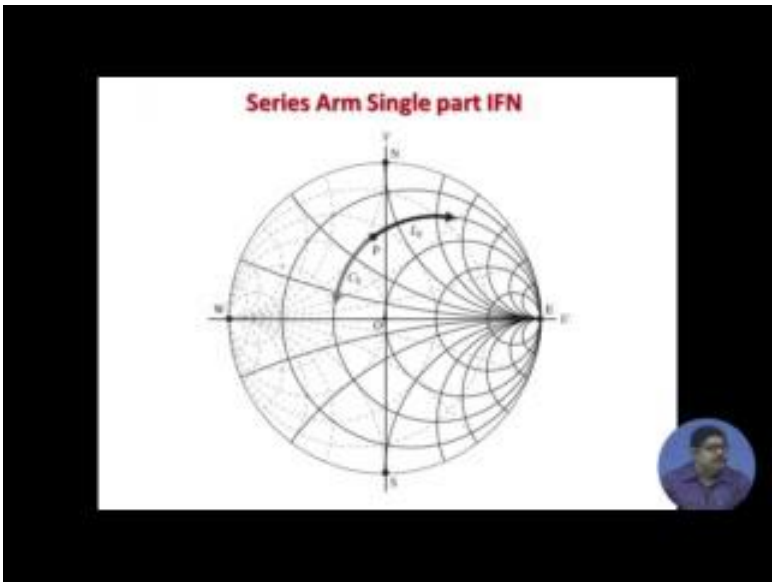

So, in the smith chart how that will vary we have seen the capacitance in previous day. So, suppose P is a point, now this point P, suppose my point with that it is before I joined the impedance matching network or before I joined the series arm. Now, I add a series thing. So, if it is a series inductor; that means, the inductance value will be more. So, positive reactance will be more. So, from that smith chat you know basically that means, I will move on the constant resistance circle, but I will move clockwise and get a higher value of reactance. On the other hand, if the series arm is a capacitor then I will come down that means, I will move in the anti clockwise direction. So, that is shown by c S direction. So, series arm makes a clockwise for a l movement anti clockwise for a c arm.

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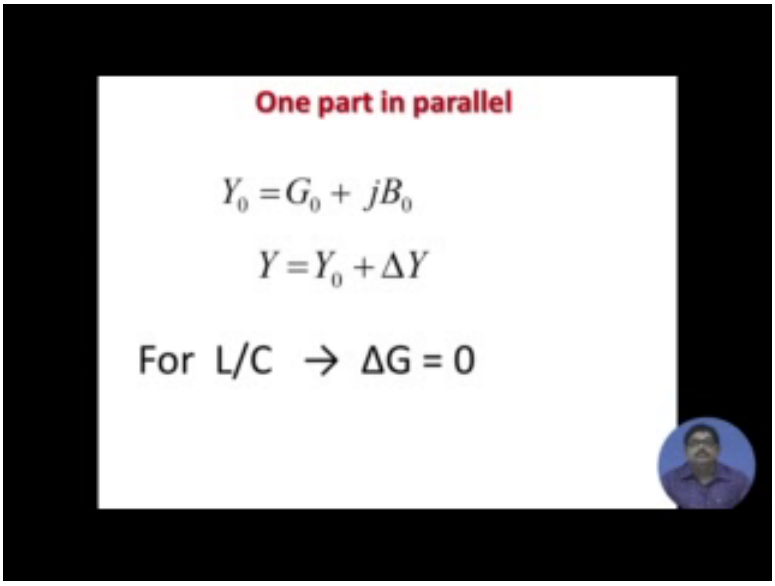


Now, similarly the branch may be in parallel in that case the new admittance will be the old admittance plus delta Y and for L and c the conductance change will be 0.

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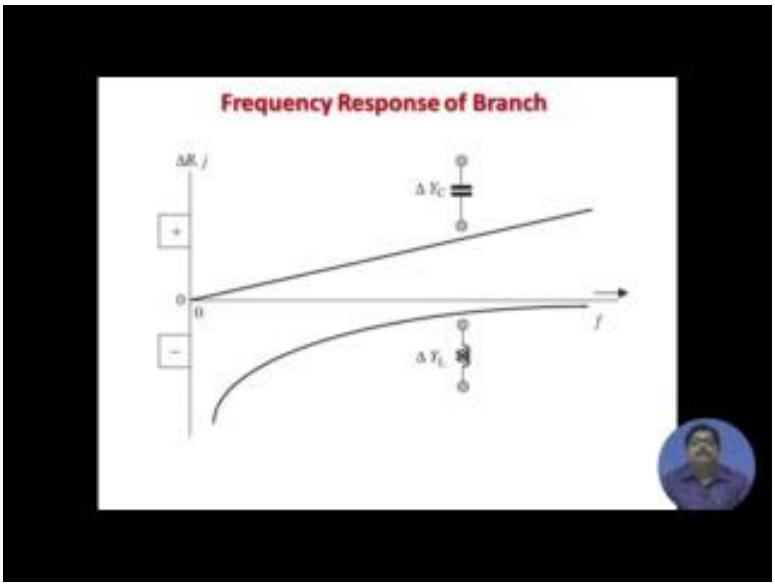


So, this is the frequency response of the branches, this also you know.

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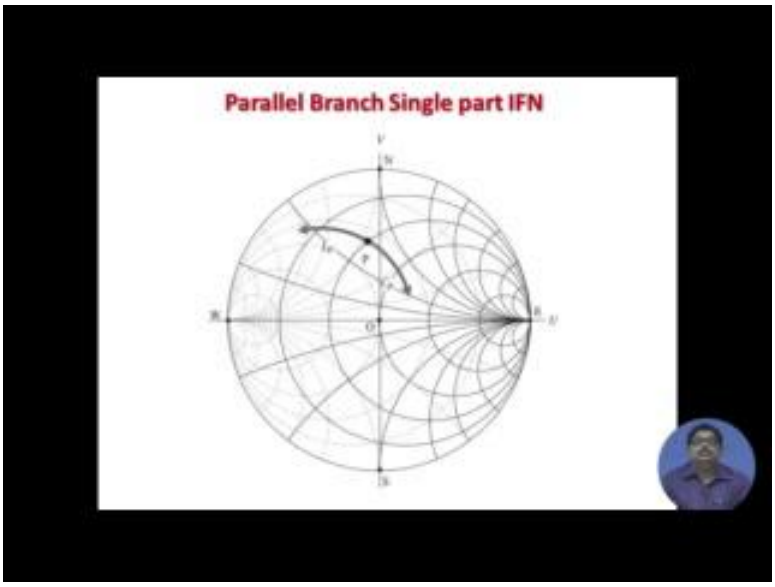


Now, in smith chart this means from the point P from this point P if I have a parallel branch of inductance. This means I am going in the anti clockwise direction whereas, for A C P parallel capacitor in parallel branch I am coming clockwise. Now, that means, that in this the previous 2 pictures I have put here. So, the point P you try to see this point is the point P. So, there is an impedance.

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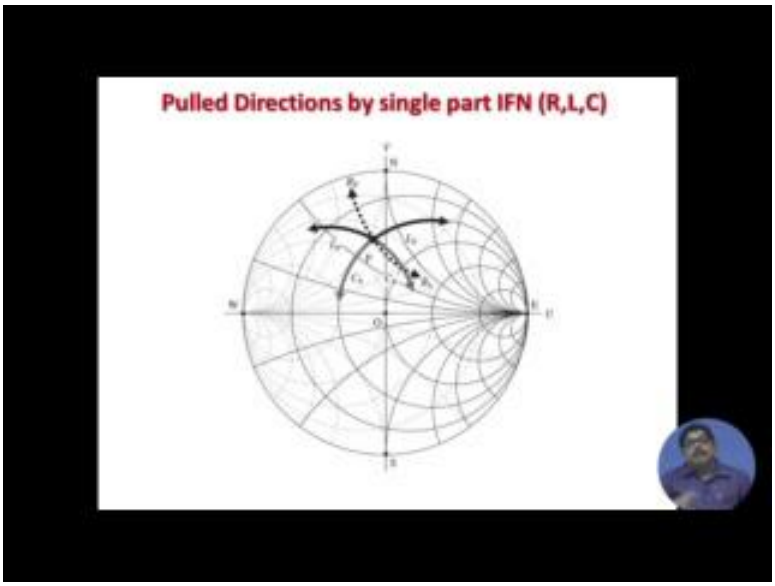


Now, the impedance matching network is either adding either an R or L or C any of them a single one. So, if it is a single element L, it is a movement in the clock wise direction, if is A C S it is in the anti clockwise direction. So, you see various pool directions here

Now, based on that the point is that from 1 point P, suppose that returned loss is not acceptable I want to come closer or lower return loss circle. So, with the help of this impedance matching network, I can be pulled to various impedances that is this diagram will help you that which 1 to add whether to add an l S R P you have various choices, but where it will be pulled you can see here and. So, you see whether that is acceptable or not etcetera whether you are getting an increase of return loss or decrease of return loss; obviously, your goal is by this pulling if you can come to the centre of the chart. So, that that will be the match that is the conjugate match case that there is no reflection there because centre of a smith chart means their reflection coefficient is zero. So, by this pulling you can come to 1 part to other.

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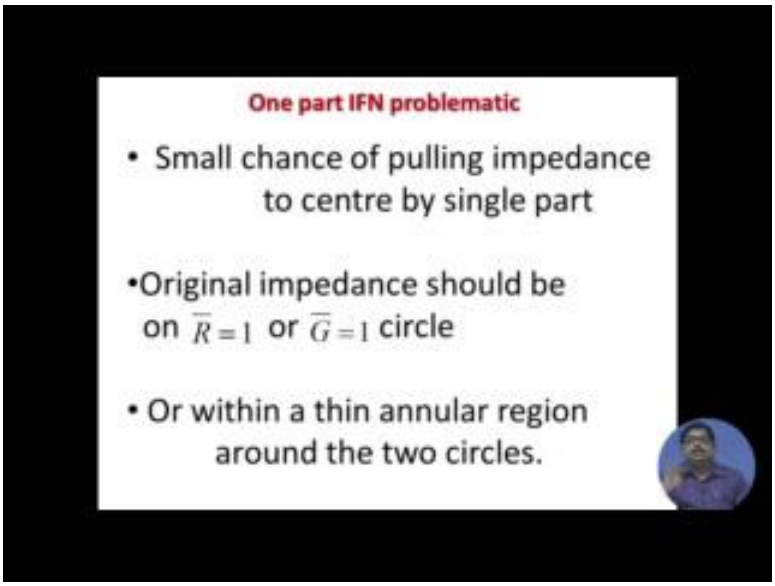


Now, 1 with a single part this impedance matching network this is problematic because small chance of pulling impedance to centre by single part because of in 1 direction you can pool by a single element original impedance should be on R is equal to 1 or G is equal to 1 circle then only you can do a perfect conjugate match with these if the original impedance is not on constant resistance constant reactant circle then by pulling alone by a single element you cannot do that, but the whole game changes if we use instead of 1 part 2 part impedance matching network.

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So, narrow band impedance matching with 2 parts is more practical generally that is called l section actually l, but to pronounce sometimes it is e l also called. So, basically in an e l section you have 1 arm 1 branch; that means, 1 series element 1 parallel element

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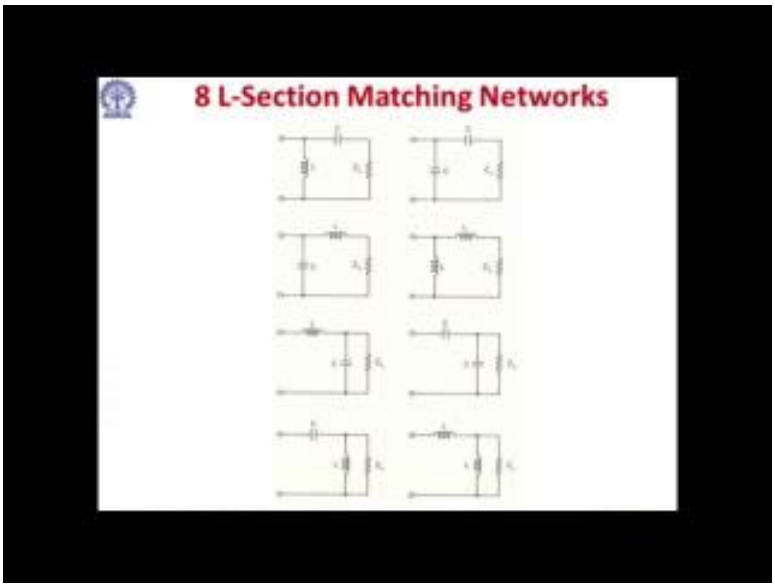


Now, there are 8 such possibilities of the l section, you see that you can have all the right side is the load. So, you have either a series c both the series and parallel; that means, the arm and branch both are C both are L the first one, l the second one, l or various combinations. So, there will be eight such combinations as I have seen here. So, 8, l section matching networks are possible from that you can choose now which 1 choose at which point for that actually the smith chart is divided into four regions.

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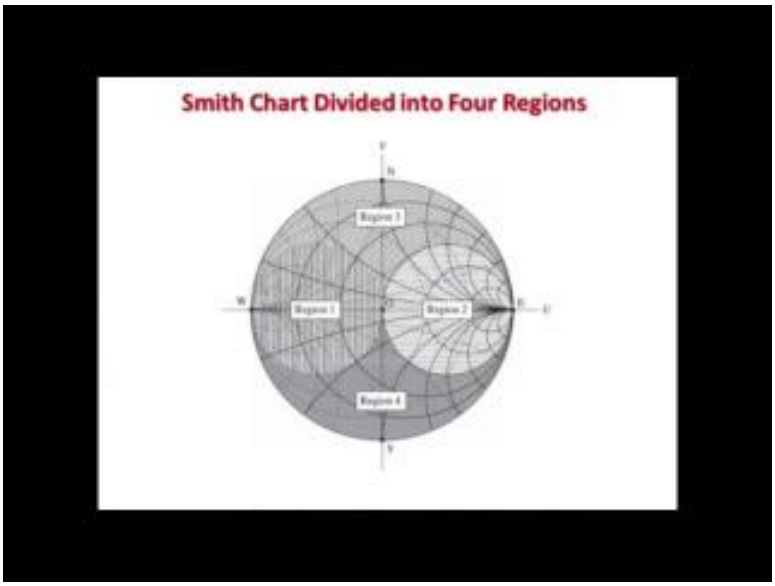


As you can see how that regions are defined all these regions suppose region one; that means, if you are having that in the admittance chart, what we call 1 plus j b that circle that; that means, the left part of the smith chart where it is passing through centre as 1 periphery and the left end of smith chart 1 periphery then if you draw that circle that is region 1, the region 2 differentiating is soon which is generally our 1 plus j b circle in the standard impedance smith chart similarly the 3 and 4, you can see.

Now, based on your original impedance that is at which point you decide these things. So, if you were your original impedance if it falls on region 1 then you will have to take 1 strategy then region 2 regions 3, region 4. So, your first impedance at which point depending on that you can choose 1 of that 8 ones.

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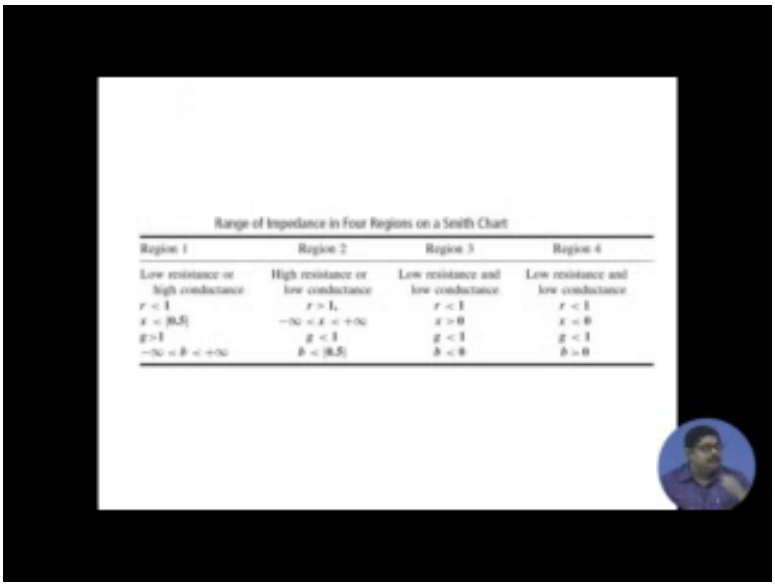


Let us proceed. So, here we have seen that these four regions on smith chart region 1 region 2 whatever we said in region 1 basically we have the R is less than 1 R means the R bar x is x bar etcetera. So, that is low resistance part region 2 is high resistance part region three is low resistance as well as low conductance and region four low resistance and low conductance. So, based on that these four regions

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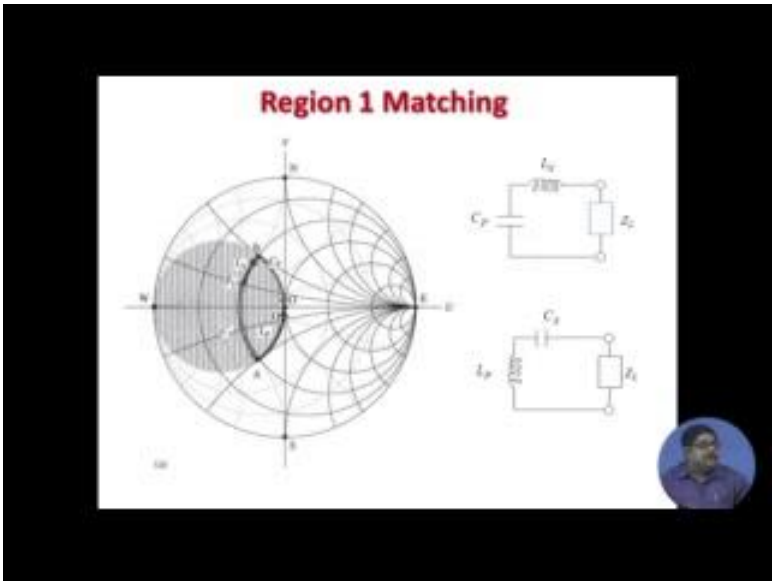


Now, this is the thing that region 1 if i am in region 1 again P now we are calling since it is region 1 P 1; that means, the original impedance is here now finally, I want to come to

the centre of the chart. So, I have 2 ways, either I can be pulled like this and then I come to the centre. So, you see again I am doing that from P 1, I will be pulled i know that by 1 element I can be pulled in various ways. So, I will be pulled from here to top. I will touch that 1 plus j b that circle it is reflected 1 this constant 1 circle and from there I will come to the centre or I can instead of that, I can also from here come like here up to this and then I can be pulled to the centre.

So, I have 2 such alternatives the first alternative now again if you go to that single part there how the pulling. So, if I want a by a single part I want a clock wise pulling I should have a l S in the series arm and then if I want a clockwise pulling that should be in a parallel branch it is a CP. So, that is why the first circuit in the right part that l S C P is my choice or the second 1 means I will have to be pulled like this. So, you can see that if I want this anti clockwise movement pulling then I need C S in the series part and 1 parallel l p. So, either this or this second 1 is my choice.

Now, it is up to you which 1 you choose we will see that the frequency responses of these 2 are generally different. So, from that you need to plot the reference and see generally the 1 rule of thumb is try to see that which 1 gives you the lower values of those l and C; that means, the disc when you are getting pulled do not get pulled by much. So, the minimum path that you can take, but still that is the rule of thumb always it is not valid more meaningful is you can always plot the frequency response and try to be as better or wide bandwidth things by choosing the 1 which gives you more.

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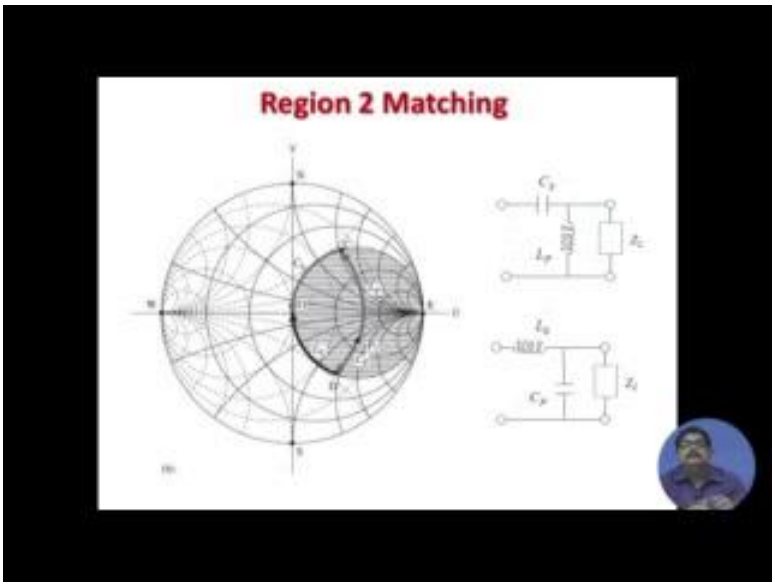


The same thing in region 2 if you are originally in region 2 that means, in point P 2 you see that in 2 ways you can be pulled from P 2 you can either come down to point d and then from d to d o or from P 2 you could have gone to c and then c to o. So, again by looking at that final graph of 1 way thing; that means, this 1 this 1 this actually helps you to tell that which 1 you are getting pulled, which element to choose from that people have already found out that for region 2 you have these 2 choices.

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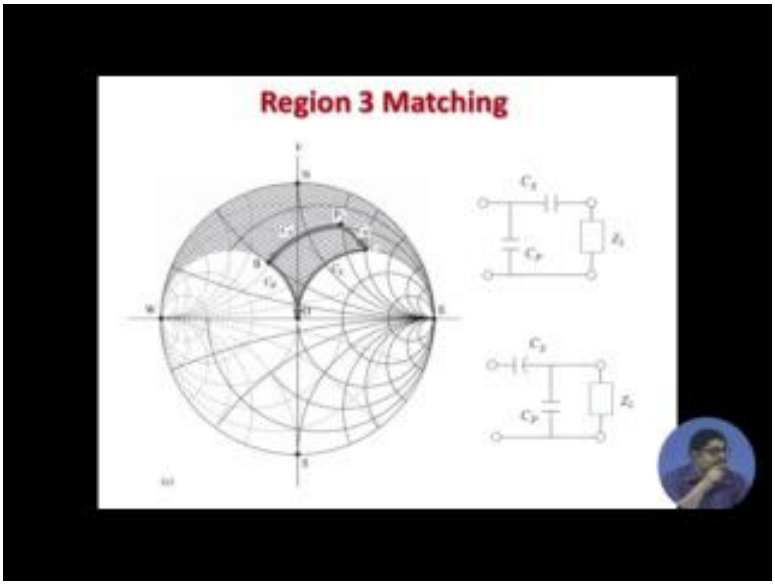

Same thing for region three you can be from P 3, you can either come to C and then to o or you can go to b and then o depending on that there are 2 choices region 2 four choices

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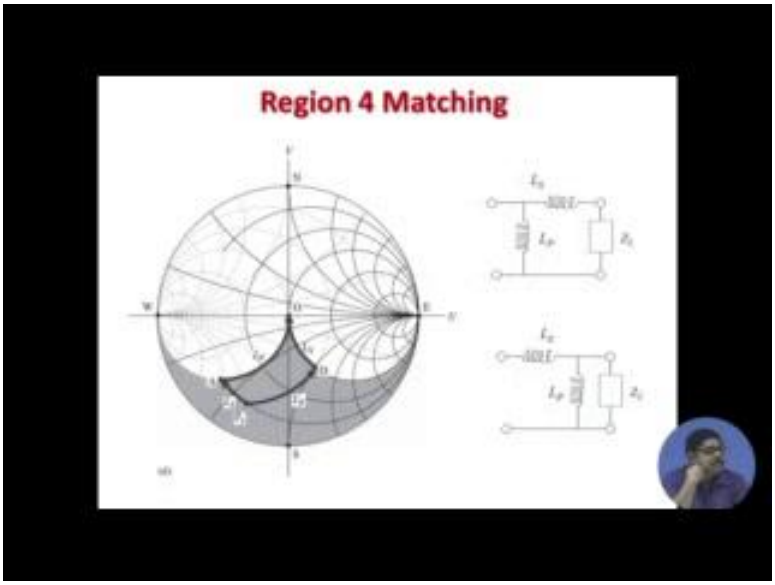


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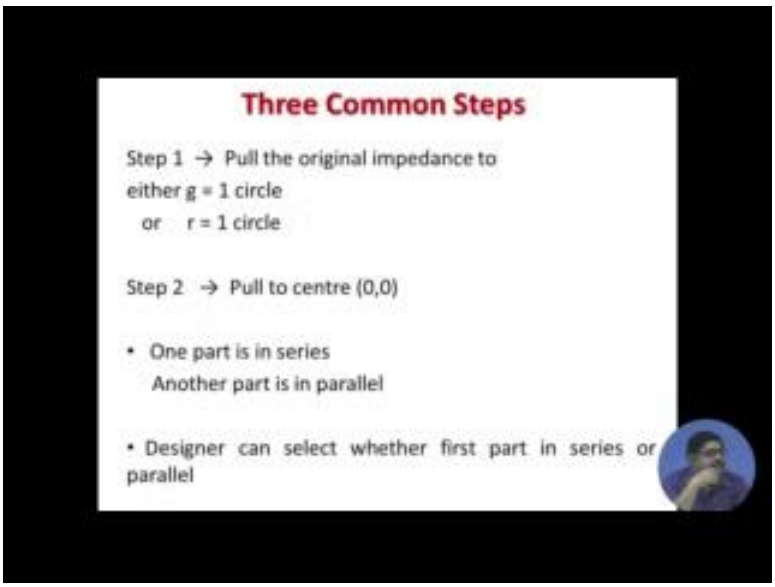


So, if you summarize the common steps in all these step 1 is pull the original impedance to either g is equal to 1 circle or R is equal to 1 circle which 1 is appropriate depending on your position then by the next part of the component you get pulled to the centre. So, the first part of the component that brings you to either R is equal to 1 or g is equal to 1 circle and the second part brings you to the centre. So, 1 part will be always in series

another part is in parallel now it is up to you to select whether the first part you want as series or parallel. So, you see all these designs whether the first one; that means, from load the first connected 1 that is in series or parallel that is your choice you see all these are different in these two, but which elements that is up to you.

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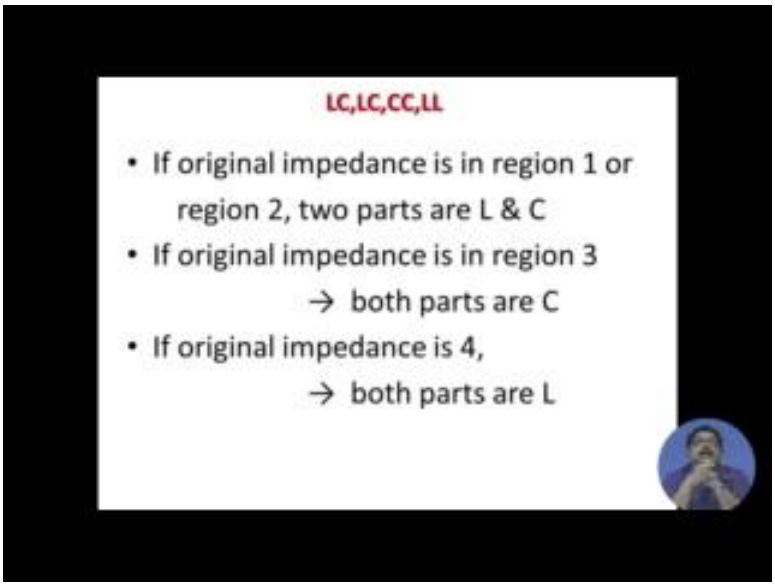


And you see that if your original impedance is in region 1 or region 2 then 2 parts 1 of them will be L and another will be C that is why I have given this heading you see LC. So, first and second region they will have your choices both the components are opposite LC whereas, if you are in region 3 then both parts are C, if original impedance is 4 then both parts are inductances.

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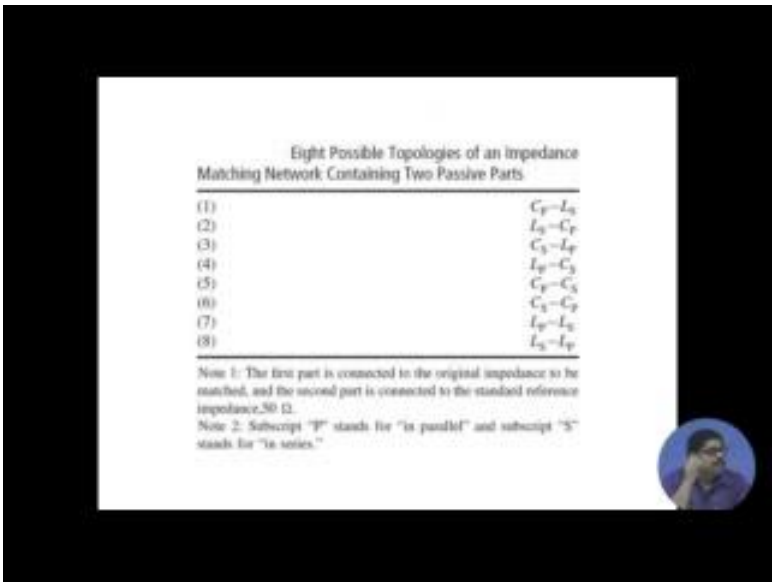


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Now, you can decide 8 possible topologies and so this you see that if you choose. So, this is another thing at in certain cases you cannot always it is not guaranteed that by this 2, 1 you can get a proper impedance matching that means, always you will be able to come to centre that is not. So, here is a list that will help you that if you are in region the first column, second column says that if you are in those regions and you choose the topology that is in the first column, then you will be able to come out, but if the third column says that if you are in region of those regions and you choose the that

corresponding topology would not be able to come out those are called prohibited regions. So, if you are in prohibited regions by that topology you cannot come out.

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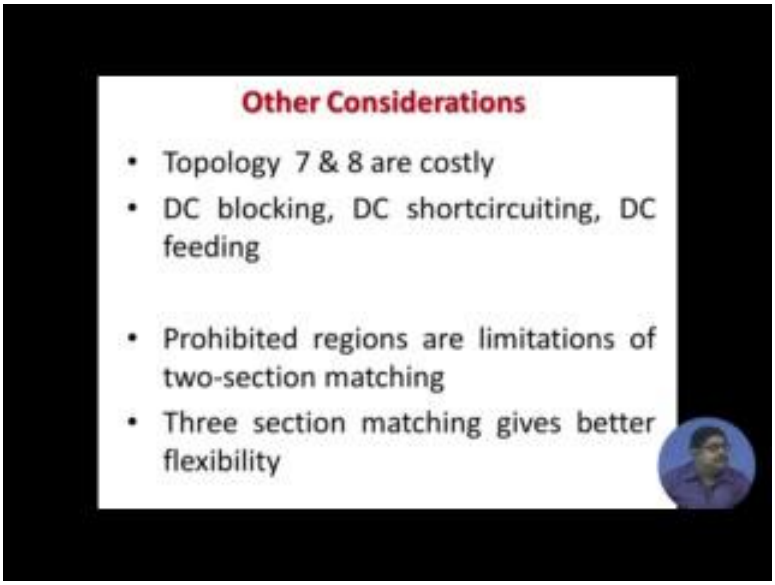


So that means, and also some other considerations is that topology 7, 8 topology, you see here 7 and 8 means both that components are inductance. Now, fabricating an inductance is difficult at high frequencies also inductances are costlier than capacitances. So, 7 and 8 generally people avoid that these are costly.

Then DC blocking, DC short circuiting, DC feeding these are also other things because capacitors sometimes are used for DC blocking etcetera. So, which one if you have do not have capacitors DC blocking may be problem etcetera l you know that if you have both ls you can have DC short circuiting etcetera. So, based on that now prohibited regions are limitations of 2 sections matching, always it is not guaranteed that you will be able to come out by any topology, but if you choose the proper topology then whatever way we have shown you would not be in the prohibited region. So, you have some choices there, but it is a limitation that by 2 parts you cannot have always a match that is why three parts are better that impedance matching network built of three parts.

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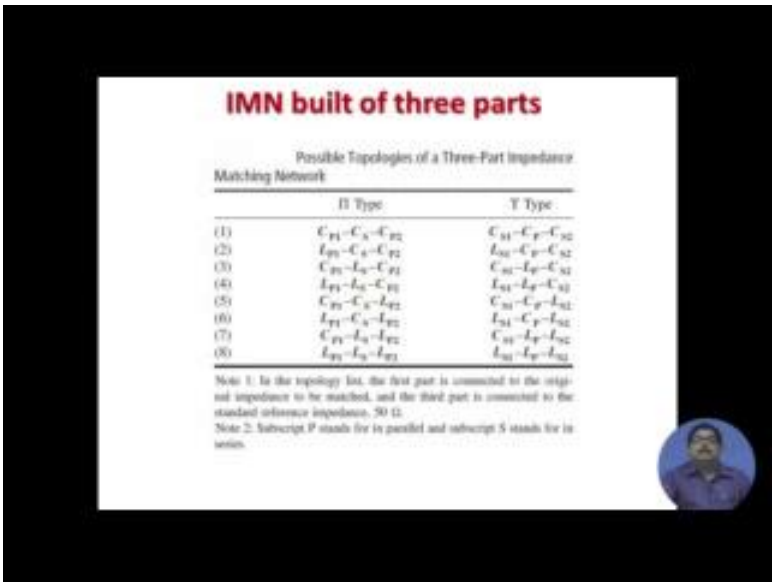


These are the all the possible topologies we have listed. We are not going here just for your reference.

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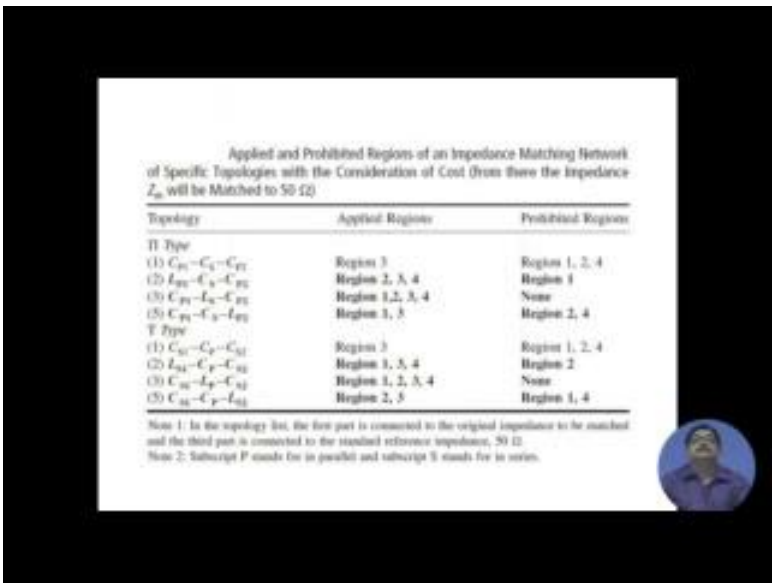


If any of you attempt it here then you can see that there are some of the cases like the topology in a number 3 and topology number 3 in both the pi type and t type there are no prohibited regions. So, all possible wherever you are in the smith chart in the original impedance always it can be matched by these topologies.

So, in this lecture we have tried to see the l section matching that means, by l c network how to do the impedance matching. So, that you can put an impedance matching network if the source and load they are not in your hand their impedances, but you want to make a conjugate match for them you can put proper LC network. So, that source will also see a that it is seeing a conjugate matched network.

Similarly, load will also see that the impedance matching network is developing giving me the conjugate matched source. So, both the power transfer can be there internally inside the impedance matching network. There may be reflections and things we are not bothered about that because our job is transport from source to load that is achieved by impedance matching network. So, this is about passive using passive components to do this matching. In the next lecture, we will see how we can use distributed components to do the same type of matching.